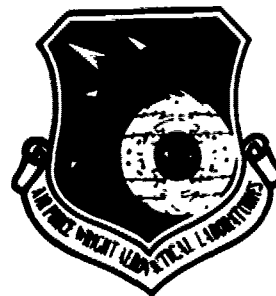# LEVEL II

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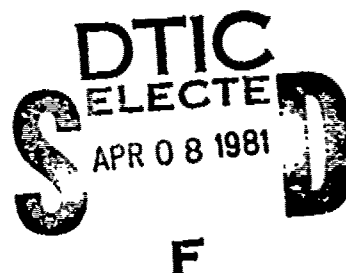CONTROLLED AVALANCHE TRANSIT-TIME TRIODE AMPLIFIERS

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Department of Electrical and Computer Engineering
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Ann Arbor, Michigan 48109

November 1980

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Collector transit-time mechanisms
Large-signal computer simulation
Controlled avalanche transit-time triode amplifiers

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The purpose of this work is to study the theoretical effects of avalanche
multiplication and collector transit time on microwave controlled avalanche
transit-time triode (CATT) devices. The objectives of this report are to
obtain a better device model, develop a complete one-dimensional large-signal
simulation computer program, calculate the large-signal performance of Class C
CATT amplifiers and make a comparison between Class C CATT and Class C BJT
amplifiers. The following studies were carried out in order to achieve these
objectives.

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20. Abstract (Cont.)

A dc computer program was developed which calculates the dc avalanche multiplication factor vs. base-collector dc bias characteristics. The results provide an estimation of the suitability of various semiconductor materials, optimum collector geometrical structures and doping densities.

Analytical models of dc and small-signal characteristics for Read-type collector structures are given which incorporate both the avalanche multiplication and collector transit-time mechanisms. Contrary to previous findings, the small-signal characteristics indicate that a large avalanche multiplication factor decreases the RF power gain of small-signal Class A CATT amplifiers. The results are given and discussed.

A large-signal computer simulation was developed which consists of three computer programs: the emitter-base computer program (EBCP), the large-signal simulation program (LSSP), and the collector circuit computer program (CCCP). The effects of high impurity doping level in the emitter, high injection level in the base, time-varying width of the neutral base region, carrier-induced drift field in the base, nonzero minority carrier concentration at the edge of the base-collector depletion region in the base, and the feedback hole current are incorporated in EBCP. Computer program LSSP models the semiconductor region through a set of difference equations of the semiconductor equations. A current-conserving boundary condition is given. The simulation includes the velocity-electric field, diffusion-electric field, and avalanche ionization rate-electric field characteristics in the collector region. The computer program CCCP incorporates the displacement current in the collector semiconductor region and the effects of the external load impedance.

Large-signal results of Class C CATT amplifiers are obtained and are presented. Effects of base-collector dc bias, load, collector structure, and operating frequency are discussed. The simulation calculates amplifier output power, gain, and efficiency. It also gives the emitter-base current and voltage waveforms; avalanche multiplication factor; waveforms of voltage across the base-collector depletion region and collector terminal current; and spatial distributions of electrons, holes, and electric field at any time instant. Large-signal output power, gain, efficiency, dynamic range, and inherent bandwidth of Class C CATT and BJT amplifiers are compared and suggestions for further studies are given.

FOREWORD

This report describes the investigation of simulation studies at the Electron Physics Laboratory, Department of Electrical and Computer Engineering, The University of Michigan, Ann Arbor, Michigan. The work was sponsored by the Air Force Systems Command, Air Force Avionics Laboratory, Wright-Patterson Air Force Base, Ohio under Contract No. F33615-77-C-1132.

The work reported herein was performed during the period July 1977 to July 1980 by Dr. Shiuh-Wuu Lee. The report was released by the author in September 1980.

The author wishes to thank Professor G. I. Haddad for his suggestion of the dissertation topic and for his guidance and helpful suggestions during the course of the investigation and Professor Nino A. Masnari for his helpful guidance and encouragement. He is also grateful to Dr. M. E. Elta and Dr. R. K. Mains for their assistance in the computer simulation program.

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LIST OF SYMBOLS

A	Ionization constant (cm^{-1}).
A_E	Effective device cross-section area in one-dimensional simulation (cm^2).
A_n, A_p	Ionization rates for electrons and holes, respectively (cm^{-1}).
B_{in}, B_{out}	Input and output susceptances as defined in Fig. 3.6.
B_L, B_S	Load and source susceptances as defined in Fig. 3.7.
$B_{L_{opt}}, B_{S_{opt}}$	Optimum load and source susceptances for maximum operating gain.
BW_{in}^i, BW_{out}^i	Device inherent bandwidths at the input and output ports as defined by Eqs. 3.76 and 3.77.
b	Ionization constant (V/cm).
$\tilde{b}_{ij}$	Small-signal susceptances as defined by Eqs. 3.54 and 3.55.
b_n, b_p	Ionization constants for electrons and holes, respectively (cm^{-1}).
C_b, C_i	Capacitors associated with the base region as defined by Eq. 4.26 (F).
C_c	Base-collector depletion capacitor (F).
C_{DE}	Emitter-base diffusion capacitor (F).
C_{DEFF}	Effective emitter-base diffusion capacitor defined by Eq. 4.21 (F).
C_L	Load capacitor (F).
C_{TE}	Emitter-base depletion capacitor (F).
D_n, D_p	Diffusion coefficients of electrons and holes, respectively $(cm^2 \cdot s^{-1})$.
D_{nEFF}	Drift field effect including effective electron diffusion coefficient $(cm^2 \cdot s^{-1})$.
d	Lateral separation between adjacent emitter and base fingers (cm).

dc	When used as a subscript of a current or current density indicates a dc quantity.
E	Electric field intensity (V/cm).
E_B	Breakdown electric field intensity (V/cm).
E_6	Electric field intensity in the high-field region of a Read-type collector structure (V/cm).
E_{sus}	Minimum electric field intensity required to sustain charge carriers at their saturation drift velocity (V/cm).
E_{sus_n}, E_{sus_p}	Minimum electric field intensities required to sustain electrons and holes at their saturation drift velocities, respectively (V/cm).
e	Electronic charge (1.6021×10^{-19}C).
f	Frequency (Hz).
f_{max}	Maximum frequency of oscillation above which operating power gain is less than or equal to 1 (Hz).
G	Avalanche generation rate ($cm^{-3} \cdot s^{-1}$).
G_{in}, G_{out}	Input and output conductances as defined in Fig. 3.6.
G_L, G_S	Load and source conductances as defined in Fig. 3.7.
$G_{L_{opt}}, G_{S_{opt}}$	Optimum load and source conductances for maximum operating gain.
G_P	Operating power gain (dB).
$\tilde{g}_{ij}$	Small-signal conductances as defined by Eqs. 3.54 and 3.55.
h, w	Widths of base fingers and emitter fingers, respectively (cm).
I	When used as a subscript indicates a difference equation field point.
I_B	Base current (A).
$I_c, I_{cc}, I_{CDE}, I_{CTE}$	Collector current, collector displacement current, emitter-base diffusion current, emitter-base displacement current, respectively (A).

$I_{c_{ns}}, I_{c_{ps}}$	Electron collector reverse saturation current and hole collector reverse saturation current, respectively (A).
I_E, I_{ET}	Emitter particle current and emitter current, respectively (A).
I_{nB}, I_{nE}	Electron current injected into the collector region and electron emitter current, respectively (A).
I_{pB}, I_{pE}	Hole feedback current from the collector region and hole emitter current, respectively (A).
I_T	Induced collector particle current (A).
J	When used as a subscript indicates a difference equation space-charge point.
$J_{subscript}$	Current density (A/cm^2).
K	When used as a superscript indicates a difference equation time point.
k	Boltzmann's constant $(1.380 \times 10^{-23} \ J/°K)$.
L_L	Load inductor.
L_n, L_p	Diffusion lengths of electrons and holes, respectively (cm).
ℓ	Length of emitter fingers (cm).
M_A, M_{A_o}	Average multiplication factor under dynamic operating conditions and dc multiplication factor, respectively.
N_A, N_D	Acceptor and donor impurity doping densities, respectively (cm^{-3}).
N_{av}, N_{drift}	Doping densities in the high and low regions of a HI-LO collector structure, respectively (cm^{-3}).
N_c	Doping density in a uniformly doped collector structure (cm^{-3}).
n	Electron density (cm^{-3}).
n_o	Thermal equilibrium electron minority carrier concentration (cm^{-3}).

n_B	Electron density at the base-collector metallurgical junction (cm^{-3}).
n_{dc}	Dc electron density (cm^{-3}).
n_i	Semiconductor intrinsic carrier density (cm^{-3}).
P_{avo}, P_{avs}	Powers available across the output terminal and the input terminal, respectively, as defined in Fig. 3.7 (W).
P_{dc}	Dc power dissipation in the collector region (W).
P_{in}, P_{out}	Input and output power (W).
p	Hole density (cm^{-3}).
p_o	Thermal equilibrium hole minority carrier concentration (cm^{-3}).
p_B	Hole density at the base-collector metallurgical junction (cm^{-3}).
p_{dc}	Dc hole density (cm^{-3}).
Q	Quality factor of the tank circuit load.
Q_B, Q_{EB}, Q_c	Charges stored in the neutral base region, on each side of the emitter-base depletion region, and in the doping clump of a LO-HI-LO collector structure, respectively.
R_B	Equivalent base region spreading resistor.
$R_b, R_{bb'}$	Resistors representing the resistances associated with the base region between adjacent emitter and base fingers and the base region directly beneath the emitter fingers, respectively.
R_L	Load resistor.
S	Linvill stability factor as defined by Eq. 3.68.
T	Temperature.
T	Time period of a cyclical quantity (s).
U	A measure of the degree of activity of amplifiers as defined in Eq. 3.66.
V_1, V_2	Voltages corresponding to the minimum and maximum points of the RF voltage across the collector depletion region, respectively (V).

$\tilde{V}_1, \tilde{V}_2$	Small-signal voltages as defined in Fig. 3.6.
$\tilde{V}_a, \tilde{V}_b$	Small-signal voltages as defined in Fig. 3.6.
$V_B, V_{BI}, V_{PT}, V_{sus}$	Junction breakdown voltage, junction built-in potential, collector punch-through voltage, and minimum voltage across the collector depletion region needed to maintain carriers at their saturation drift velocity at all times, respectively (V).
$V_{bias}, V_{sig}, \tilde{V}_{sig}$	Base-collector dc bias, emitter-base input signal, and small-signal emitter-base input signal, respectively (V).
$V_{EB}, V_{EBJ}, V_{CB}, V_L, V_T$	Voltages across the emitter-base terminal, emitter-base depletion region, base-collector junction and the load, the load, and the base-collector depletion region, respectively (V).
v_n, v_p	Drift velocities of electrons and holes, respectively ($cm \cdot s^{-1}$).
v_{ns}, v_{ps}	Saturation drift velocities of electrons and holes, respectively ($cm \cdot s^{-1}$).
v_s	Carrier saturation drift velocity ($cm \cdot s^{-1}$).
w_1, w_2, w_3	Boundaries of depletion regions as defined in Fig. 3.1.
w_{av}, w_D	Widths of the high and low doping regions of a HI-LO collector structure, respectively (cm).
w_B, w_{B_o}	Width of neutral base region and separation between emitter-base and base-collector metallurgical junctions, respectively (cm).
w_c	Width of high doping region of a LO-HI-LO collector structure (cm).
w_E, w_{E_o}	Width of neutral emitter region and depth of the emitter-base metallurgical junction, respectively (cm).
w_T	Width of the whole collector region (cm).
$w_{V_{sus}}$	Collector depletion width when $V_T = V_{sus}$.
x, y	Space coordinates in the collector region and the base region, respectively (cm).

xxi

x_{B_1}, x_{B_2}	Width of base region beneath the emitter finger and the depth of emitter-base metallurgical junction from the device surface, respectively (cm).
Y_{in}, Y_{out}	Input and output admittances, respectively.
Y_L, Y_S	Load and source admittances, respectively.
y_{ij}	Device small-signal y-parameters defined by Eqs. 3.48 and 3.49.
$\bar{y}_{ij}$	Device small-signal y-parameters defined by Eqs. 3.54 and 3.55.
Z_L	Load impedance.
0	When used as a subscript of a voltage or an electric field quantity indicates a dc quantity.
1	When used as a subscript for a current, a voltage or an electric field quantity represents a small-signal RF quantity.
α	Ionization rates (cm^{-1}).
α_o	Dc ionization rates (cm^{-1}).
α_o	Dc common-base current gain.
$\alpha_{inj_o}, \alpha_{t_o}$	Dc emitter injection efficiency and dc base transport factor, respectively.
β_o	Dc common-emitter current gain.
δ	Amplifier input tunability.
ε	Dielectric permittivity ($F \cdot cm^{-1}$).
η	Amplifier efficiency (percent).
η_c	Collector dc to ac conversion efficiency (percent).
θ_D, θ_T	Transit angles of the drift region and the whole collector, respectively.
$\theta_{inj}, \theta_{sc}$	Phase angles associated with charge injection and delay of charge injection due to space charge, respectively.
μ_n, μ_p	Electron and hole mobility, respectively.

ρ Resistivity ($\Omega \cdot cm$).

σ_B Conductivity in the base region ($mho \cdot cm^{-1}$).

τ_e Delay time in responses due to heavy impurity doping level in the emitter region.

τ_g Transit time in the carrier generation region.

τ_n, τ_p Lifetimes of electron minority carriers and hole minority carriers in p- and n-type semiconductors, respectively (s).

τ_R Dielectric relaxation time.

$\dot{\psi}$ Potential variation in p-n junction depletion region.

CHAPTER I. INTRODUCTION

1.1 Historical Background

1.1.1 Bipolar Junction Transistors (BJTs).

Of all
semiconductor devices the BJT, an acronym for bipolar junction transistor,
is the most important. Its invention brought about an unprecedented
growth of research and development in solid-state physics and engineer-
ing. Transistors are now key elements, for example, in high-speed
computers, in space vehicles and satellites, and in all modern
communication and power systems.

The development of point-contact transistors by Bardeen and
Brattain[1] was announced in 1948. Then in 1949, Shockley[2] proposed a
junction bipolar transistor and laid out the basic theory of this
fundamental structure. In the microwave power bipolar transistor area,
pioneering work was done by Early[3] and Pritchard,[4] where they considered
high-frequency effects, and Ebers and Moll,[5] Fletcher,[6] and Emeis et al.,[7]
who studied high-power effects on transistor operation. Some papers
have been devoted to the analysis of the mutual dependence of these
effects.[8-10] On the other hand, some more recent studies have been
published concerning the theory and characterization of microwave
bipolar transistors.[11-15]

At the inception of the BJT, transistors were able to operate
at frequencies up to a few hundred kHz only and the chioce of the semi-
conductor material was restricted to germanium, since the material had
been produced with sufficient purity and in single-crystal form. Theory

predicted that they should be able to operate at much higher frequencies, even into the microwave frequency range, by a reduction of their overall dimensions. In particular, it was recognized that the transit time of charge carriers through the device and the rate of change of electrical charge stored within the device would limit the frequency response. In order to improve the performance at higher frequencies, the base width of the BJT must be reduced to reduce the transit time and the active device area must decrease in order to reduce the capacitance or stored charge. These refinements demanded a much tighter control on all three dimensions of the device. Transistor technology has enjoyed many break-throughs, particularly in the alloy-junction[16] and grown-junction tech-niques[17] and in zone-refining,[18] diffusion,[19-21] epitaxial,[22] planar,[23] beam-lead,[24] and ion implantation technologies.[25] These breakthroughs have helped to increase the power and frequency capabilities of transis-tors, as well as their reliability, by many orders of magnitude.

With the present technology and without electron-beam or x-ray exposure (i.e., ~ 1 um linewidth), an aspect ratio of ~ 20:1 is theoretically attainable with interdigitated, overlay or mesh structures. The practical limit, however, seems to be approximately 10:1. As to the base layer width, the lowest value achieved under a compromise between minimum base transit time and minimum base spreading resistance is ~ 0.1 µm.

The physical properties of the semiconductor theoretically determine the ultimate electrical performance of the transistor. For example, Johnson showed[8] that the maximum frequency of operation will be proportional to $E_B v_s$, where E_B is the junction breakdown electric field and v_s is the scattering limited carrier drift velocity. As the

size of the device is reduced to achieve high-frequency performance,

the voltage must be maintained at a value sufficient to give the required

power output. In the limit, a further reduction in device dimension

parallel to the electric field direction would be impossible because the

electric field would exceed E_B. In practice, the frequency limit derived

by Johnson has not been reached. For technological reasons, Si is pre-

ferred to Ge and GaAs for microwave bipolar transistors. The techno-

logical superiority of Si is due mainly to the ability of silicon dioxide

to act as a diffusion mask and the ability to etch very fine patterns

in this oxide. The oxides of Ge and GaAs are not as stable as silicon

dioxide and for these **semiconductor materials chemical vapor deposited**

silicon dioxide and silicon nitride, when used as a diffusion mask or

as an insulating material, produced results inferior to thermally grown

silicon dioxide on silicon. Much progress in GaAs technology has been

achieved in the last few years. Another reason why Si material is

preferred is its good thermal conductivity which is a factor of two

better than GaAs. Good thermal conductivity is an important concern,

especially in high-power applications.

Bipolar junction transistors have the following advantages which

assure their place in the microwave power semiconductor device family:

1. Due to their three-terminal configuration, their application,

particularly as amplifiers or switching devices, is much easier and

the corresponding circuits much simpler than for two-terminal devices.

2. Due to their operation with both majority- and minority-carrier

types, very high local current density can be reached, much higher than

in the majority-carrier devices.

3. The operating power efficiency is high, particularly for Class
C amplifiers.

4. The operational bandwidth is large, particularly for Class A
amplifiers.

5. The power gain in amplifier operation is relatively high.

6. Signal distortion is lower than in two-terminal devices. Noise
level is lower than in avalanche diodes.

7. With present Si technology, good output power can be obtained
in the X-band frequency range.[26]

1.1.2 Controlled-Avalanche Transit-Time Triode (CATT) Devices.

Diodes, and in particular the IMPATT, which is an acronym for impact
ionization avalanche transit time, have relatively simple configurations
and operate close to the well-known Johnson[8] material parameter limi-
tation. Transistors, however, perform well below the material limit,
in spite of considerable effort to optimize their configurations and
the great advancement made in Si technology. On the other hand, three-
terminal devices have many advantages over diodes as mentioned previously.
A new three-terminal device was proposed by Yu et al.[27] in 1974. This
new device was named CATT, an acronym for controlled-avalanche transit-
time triode. It is self-evident from its name that this device utilizes
both avalanche multiplication and transit time. In designing a BJT
device, avalanche multiplication has always been associated with junction
breakdown and was always avoided in amplifier applications. Incorpo-
ration of avalanche multiplication into the BJT device is important for
several design applications.[28-30] For a large number of circuits,
transistor junction breakdown is used to provide a reference voltage.

An ability to model such operation is desirable. For other applications, circuit performance under surge conditions must be determined. Possible malfunctions due to second breakdown can only be determined if an avalanche model is first established. Another reason for investigating avalanche multiplication is that when a BJT is biased in the avalanche multiplication region, a negative differential resistance between collector and emitter may exist. This part of the characteristic, commonly named the avalanche region, may be used for fast switching applications.[31] In power amplifier applications, it has been established that BJTs having long collector regions, i.e., large junction breakdown voltages, can be desirable, but it was not until the discovery of the CATT device by Yu et al.[27,32-34] that both avalanche multiplication and collector transit time were actively used to advantage in power amplifiers. In 1974, Winstanley and Carroll[35] proposed the IMPISTOR, a transistor with an IMPATT-like collector region, for which Yu et al. have suggested the name CATT. Carroll[36] discussed three possible modes of operation for the avalanche transit-time transistor: (1) the multiplication mode, (2) the negative impedance mode, and (3) the pulse mode. The modes move progressively through the phenomena of avalanche multiplication, IMPATT negative conductance combined with multiplication, and voltage collapse and high current pulses associated with TRAPATT operation. The multiplication mode will be studied in this report. Quang,[37] in 1975, presented a lumped-distributed small-signal equivalent circuit for an IMPISTOR in the negative impedance mode. In 1976, Lefebvre et al.[38] utilized a computer program developed for high-efficiency IMPATT diodes to investigate the influence of a thermionic-type injected current on the dynamic operating conditions and performance of GaAs

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IMPATT diodes. The work showed that interesting results can be obtained in X-band and the practical realization of such a device would be possible by using a CATT operating in the negative impedance mode.

1.2 Basic Properties of CATT Devices

1.2.1 Collector Structures of CATT Devices. The various structures are described in terms of the avalanche region width w_{av}, the avalanche region doping density N_{av}, the drift region doping density N_{drift}, and the drift region width w_D. The LO-HI-LO doping profiles also include the total concentration of carriers in the charge clump per unit area Q_c. The doping and electric field profiles for various common CATT collector structures are shown in Fig. 1.1 along with the parameters that are used to describe their characteristics.

1.2.2 Principles of Operation of CATT Devices. The CATT device operates in a manner similar to that of a bipolar junction transistor. In an n-type CATT device, whose structure is shown in Fig. 1.2, electrons and holes are injected across the forward-biased emitter-base junction. The majority of the injected electrons, minority carriers in the base region, diffuse across the neutral base region and then the electric field, set up by the base-collector reverse bias, draws them into the collector region. A small percentage of the emitter-injected electrons are lost in the base region through carrier recombination. Electrons that are drawn into the collector region first undergo avalanche multiplication in the high-field portion of the collector region and then drift across the depleted low-field portion. While making a transit across the collector depletion region, a current is induced at the collector terminal. Unlike the bipolar junction transistors whose

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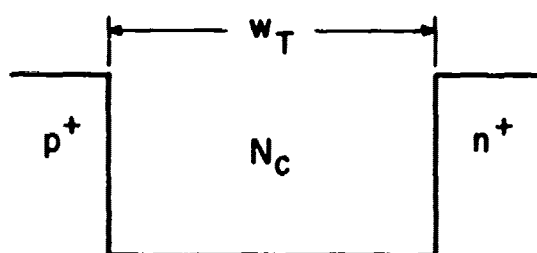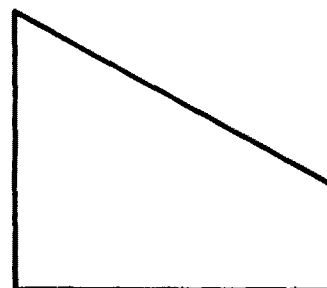
DOPING PROFILE   **ELECTRIC FIELD PROFILE**

(a) UNIFORM STRUCTURE
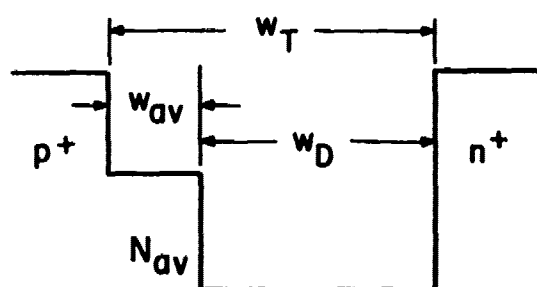
DOPING PROFILE   **ELECTRIC FIELD PROFILE**

(b) HI-LO STRUCTURE
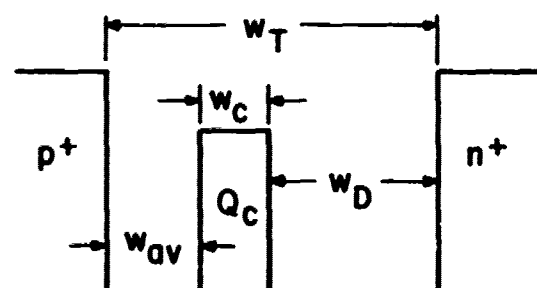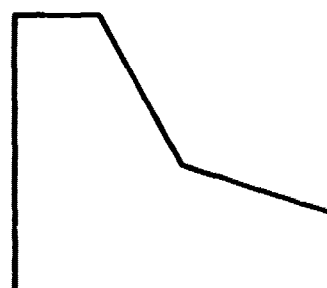
DOPING PROFILE   **ELECTRIC FIELD PROFILE**

(c) LO-HI-LO STRUCTURE

FIG. 1.1 DOPING AND ELECTRIC FIELD PROFILES OF VARIOUS CATT

COLLECTOR STRUCTURES.
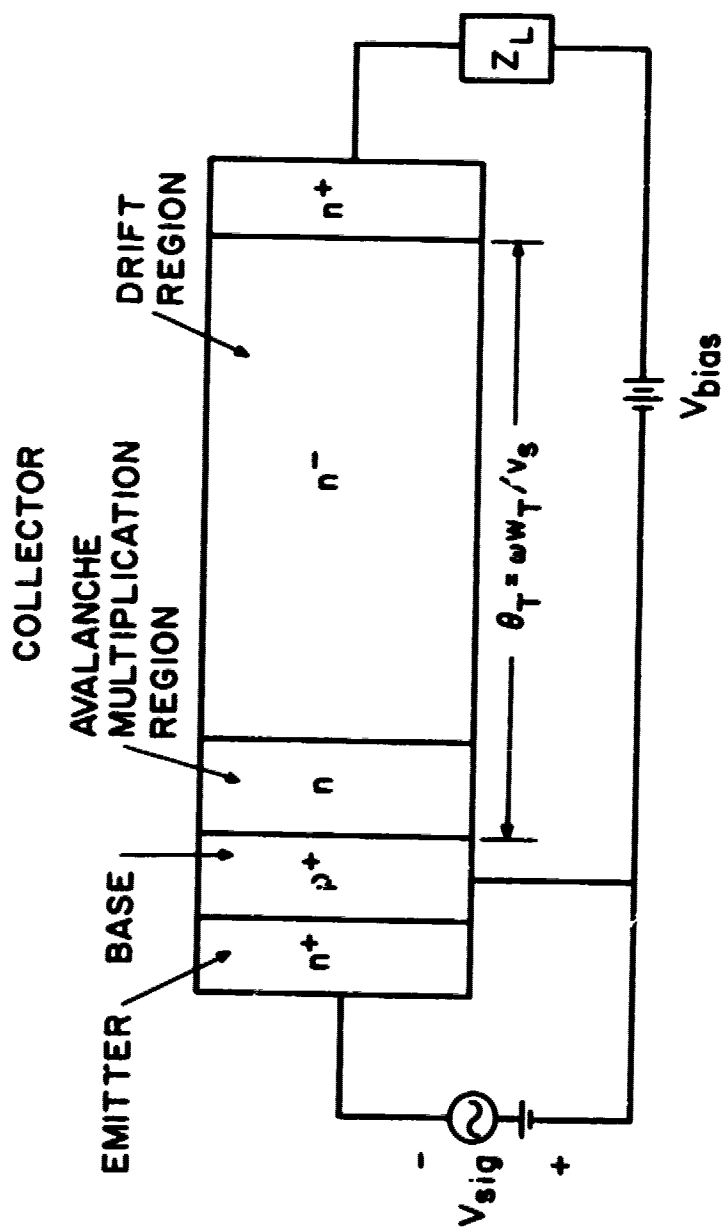
FIG. 1.2 SCHEMATIC STRUCTURAL DIAGRAM OF A CATT DEVICE.

common-base current gain is always less than unity, carrier multiplication
in the CATT device results in a current gain of the order of two to ten.
With the proper doping profile, a long collector structure allows the
sustenance of a very large RF voltage across the collector depletion
region. The CATT amplifiers develop additional power gain through ava-
lanche multiplication and by the use of transit time in the collector.
Consequently, the power gain can be much higher than for a bipolar
junction transistor having an equivalent emitter-base structure, or for
the same gain at a higher frequency.

Structurally, the n-type CATT device is similar to an npn bi-
polar junction transistor except for two major differences, as shown in
Fig. 1.2. The collector has a high-field avalanche multiplication
region in which the emitter injected electrons are multiplied and a
long drift region. It should be noted that the long drift region is
used to provide proper timing for the avalanche multiplication of the
emitter injected electrons, besides providing the collector with a
large RF voltage capability. If the load impedance is a high-Q tank
circuit whose resonant frequency equals the emitter-base signal fre-
quency, the induced current waveform of a common-base Class C CATT
device is such that its fundamental component is automatically π rad
out of phase with the near-sinusoidal collector RF voltage regardless
of the collector transit angle θ_T. The induced current waveform is
always centered around the phase angle $3\pi/2$ rad of the RF voltage wave-
form. On the one hand, if the collector region is narrow, the induced
current waveform will be narrow and the collector efficiency, which is
defined as the ratio of signal power to dc input, is high. On the

other hand, the emitter injected electrons will enter the avalanche multiplication region at a time when the voltage across the collector region is low and not many electron-hole pairs will be generated. Limited by a narrow induced current waveform and small current multiplication, a CATT device with a narrow collector region will not be able to produce very much RF power. If the collector transit angle is greater than π rad, the emitter injected electrons will enter the avalanche multiplication region at a time when the voltage across the collector region is high and carrier multiplication will be large. A collector transit angle greater than π rad implies that there is conduction current flowing during the positive half-cycle of the collector RF voltage which means energy dissipation instead of power generation. The collector efficiency is poor for large collector transit angle situations. An optimum operating condition seems to be when the collector transit angle is approximately π rad.

It should be noted that the collector RF voltage is initiated by the entering of emitter injected electrons into the collector. This is because the bias voltage, as seen by the collector, drops when the collector current flows in the external load, whereas in the IMPATT diode, the current waveform is initiated by the device voltage which is the superposition of a large RF voltage over a dc bias which is only slightly below the device junction breakdown voltage. If the space-charge effect is ignored, theoretically, a pulse of charge is always injected into the low-field drift region at the time when the phase angle of the IMPATT RF voltage is close to π rad, regardless of the drift region transit angle. The collector voltage and induced current

-10-

waveforms of a CATT device and those of an IMPATT are very similar when the drift region transit angle is approximately π rad and they are different when the drift region transit angle differs significantly from π rad.

The upper limit on the collector voltage is approximately the base-collector junction breakdown voltage V_B. Actually, the collector voltage can exceed V_B slightly for a short duration of time. The lower limit on the collector voltage is the voltage needed to sustain electrons at approximately the scattering limited velocity during its entire transit across the depleted collector region. For high-power applications, the optimum base-collector dc bias is such that the collector can have a large avalanche multiplication factor and a large RF voltage simultaneously. If the dc bias is increased above the optimum value, although the current gain would be increased, the amplitude of the collector RF voltage will be decreased due to the upper limit set by V_B. If the dc bias is decreased below the optimum value, current gain would definitely be decreased and possibly the amplitude of the collector RF voltage would also decrease due to the lower limit set by the voltage required to maintain carriers at the scattering limited velocity. At optimum dc bias, the avalanche multiplication factor of a typical CATT device ranges from two to ten rather than a million as in the IMPATT diode. Therefore, when the emitter is not injecting carriers into the collector, the collector current equals approximately ten times the thermally generated reverse saturation current. A significant conduction current exists in the collector only when the emitter-base junction is forward biased. This is why it is called a controlled-avalanche transit-time triode.

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The CATT is a complicated device for several reasons. The seemingly simple avalanche multiplication process as employed, for example, in avalanche photodiodes[39] becomes much more complex in CATT devices due to the large RF voltage swing. The CATT is complex for another reason. The avalanche multiplication generated holes will feed back into the base region and constitute a negative recombination base current component. This phenomenon results in a more uniform emitter current injection and better use of the emitter finger area than for bipolar junction transistors. If the feedback hole current is large enough the polarity of the base current is reversed. Pinch-in phenomena rather than pinch-out phenomena in the base region would occur if the carrier multiplication is large.

When the collector transit angle equals π rad, the signal carriers are injected at or near the time when the RF voltage equals V_{T_o}, where V_{T_o} is the average value of the base-collector terminal voltage, if the space-charge effect is negligible; the avalanche multiplication process is, therefore, almost independent of the RF voltage amplitude. This is an essential condition for a linear amplifier. It should also be pointed out that nonlinearity in the CATT is due mainly to the exponential turn on of the emitter-base junction as in the BJT. To a certain extent this nonlinearity is alleviated in the CATT due to the fact that the space charge will cause the effective avalanche multiplication to decrease as the input signal level is increased. This leads to a wider dynamic range.

1.2.3 Comparison of Collector Efficiencies in BJT, CATT and IMPATT Devices. For the induced collector current and voltage waveforms

-12-

shown in Fig. 1.3, denoted by I_T and V_T, respectively, the output power is given by

$$P_{out} = \frac{1}{2\pi} \int_0^{2\pi} I_T(\omega t) V_{RF} \sin \omega t \, d\omega t \qquad (1.1)$$

or

$$P_{out} \approx \frac{I_{Tmax} V_{RF}}{2\pi} [\sin(\theta_{inj} + \theta_T) - \sin \theta_{inj}] \quad , \qquad (1.2)$$

where V_{RF} is the amplitude of the collector RF voltage, I_{Tmax} is the maximum induced collector current level and θ_{inj} is the phase difference between the injected current pulse and the collector RF voltage. The dc collector current level can be found by averaging the induced current level as follows:

$$I_{T_{dc}} = \frac{1}{2\pi} \int_0^{2\pi} I_T(\omega t) \, d\omega t$$

$$= I_{Tmax} \frac{\theta_T}{2\pi} \quad . \qquad (1.3)$$

By using Eqs. 1.2 and 1.3, the collector efficiency can be expressed as

$$\eta_c = \frac{P_{out}}{P_{dc}}$$

$$= \frac{V_{RF}}{V_{T_o}} \frac{\sin(\theta_{inj} + \theta_T) - \sin \theta_{inj}}{\theta_T} \quad , \qquad (1.4)$$

-13-
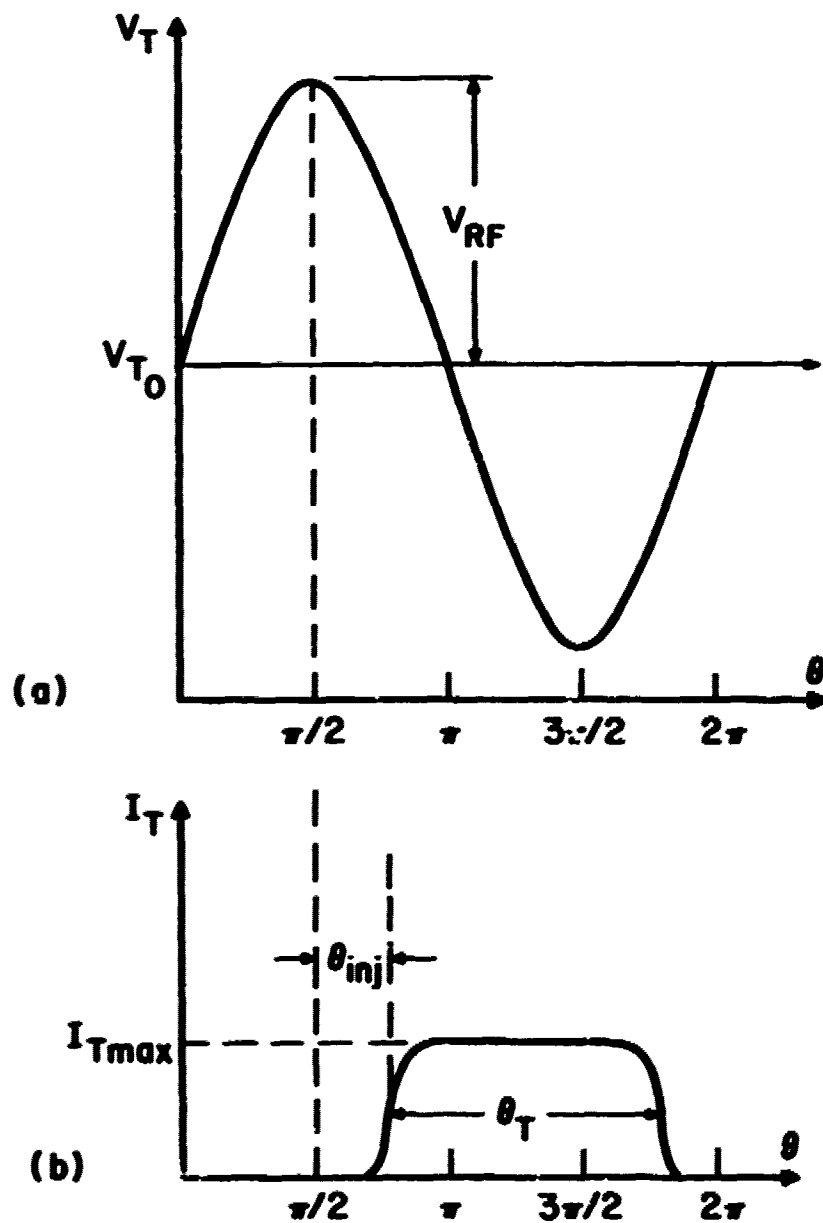
FIG. 1.3 VOLTAGE AND CURRENT WAVEFORMS IN THE CATT DEVICE.

(a) BASE-COLLECTOR TERMINAL VOLTAGE AND (b) INDUCED

EXTERNAL CURRENT.

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where P_{dc} is the dc input power. The waveforms of V_T and I_T for BJT, CATT and IMPATT devices are shown in Fig. 1.4. A negative P_{out} implies that RF power is being generated. Both the BJT and CATT devices are operating in Class C configuration and the load is a high-Q tank circuit whose resonant frequency is approximately equal to the signal frequency. The induced current waveform for the BJT is a short current pulse, because its collector region is narrow. A narrow collector region also implies that only a small RF voltage swing is allowed. From the induced current waveforms, it is expected that the CATT efficiency will be lower than that of the BJT due to the large transit angle requirement. The induced current waveforms of the CATT and IMPATT corresponding to various drift region transit angles are shown in Fig. 1.4 The maximum induced current level is assumed to be constant. For the CATT, θ_{inj} is always given by

$$\theta_{inj} = \pi - \frac{\theta_T}{2} \qquad (1.5)$$

and Eqs. 1.2 and 1.4 become

$$P_{out} = - \frac{I_{Tmax} V_{RF}}{\pi} \sin \frac{\theta_T}{2} \qquad (1.6)$$

and

$$\eta_c = - \frac{V_{RF}}{V_{T_0}} \frac{\sin(\theta_T/2)}{\frac{\theta_T}{2}} . \qquad (1.7)$$

For the IMPATT, θ_{inj} is given by
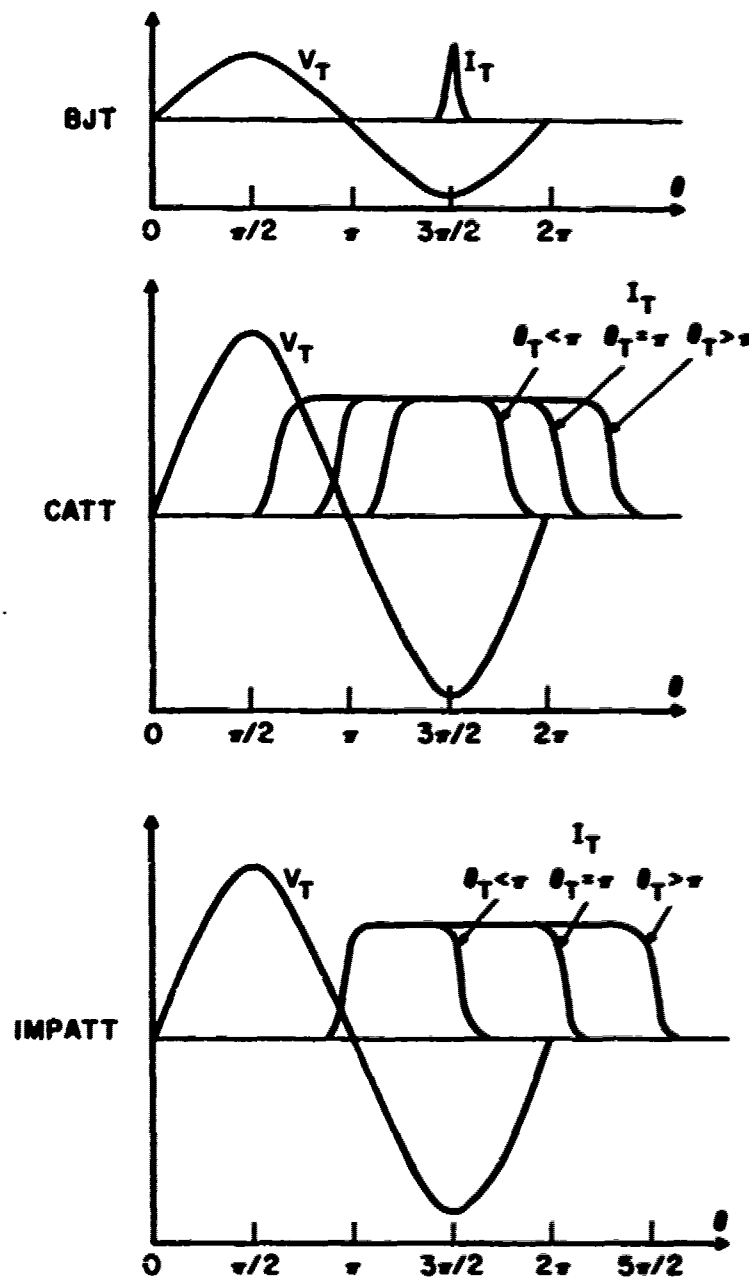
FIG. 1.4 COLLECTOR RF VOLTAGE AND INDUCED CURRENT WAVEFORMS
OF BJT, CATT AND IMPATT DEVICES.

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$$\theta_{inj} = \frac{\pi}{2} - \theta_{sc} \quad , \tag{1.8}$$

where θ_{sc} is the injection phase delay due to the space-charge effect. If the space-charge effect is ignored, $\theta_{sc} = 0$ rad and Eqs. 1.2 and 1.4 become

$$P_{out} \cong - \frac{I_{Tmax} V_{RF}}{2\pi} (1 - \cos \theta_T) \tag{1.9}$$

and

$$\eta_c = - \frac{V_{RF}}{V_{T_o}} \frac{1 - \cos \theta_T}{\theta_T} \quad . \tag{1.10}$$

Shown in Figs. 1.5 and 1.6 are plots of P_{out} and η_c as functions of θ_T at different values of θ_{inj}. The quantities of P_{out} and η_c are normalized in terms of $I_{Tmax} V_{RF}/\pi$ and V_{RF}/V_{T_o}, respectively. Results indicate that the CATT P_{out} and η_c are higher than the IMPATT due to the fact that the induced current waveform of the CATT is always centered at $\theta = 270$ degrees. It is also noticed that the CATT 3-dB P_{out} and η_c bandwidths are wider than the IMPATT. As θ_{inj} decreases due to the space-charge effect, the IMPATT normalized P_{out} and η_c and their 3-dB bandwidths also decrease.

1.3 State of the Art of BJT and CATT Amplifiers

Electrical characteristics and performance of microwave power transistors depend first on the operational mode, i.e., amplifier, oscillator, and switching, and second on the operational class, generally Class C or A, in the amplifier and oscillator cases. On the other
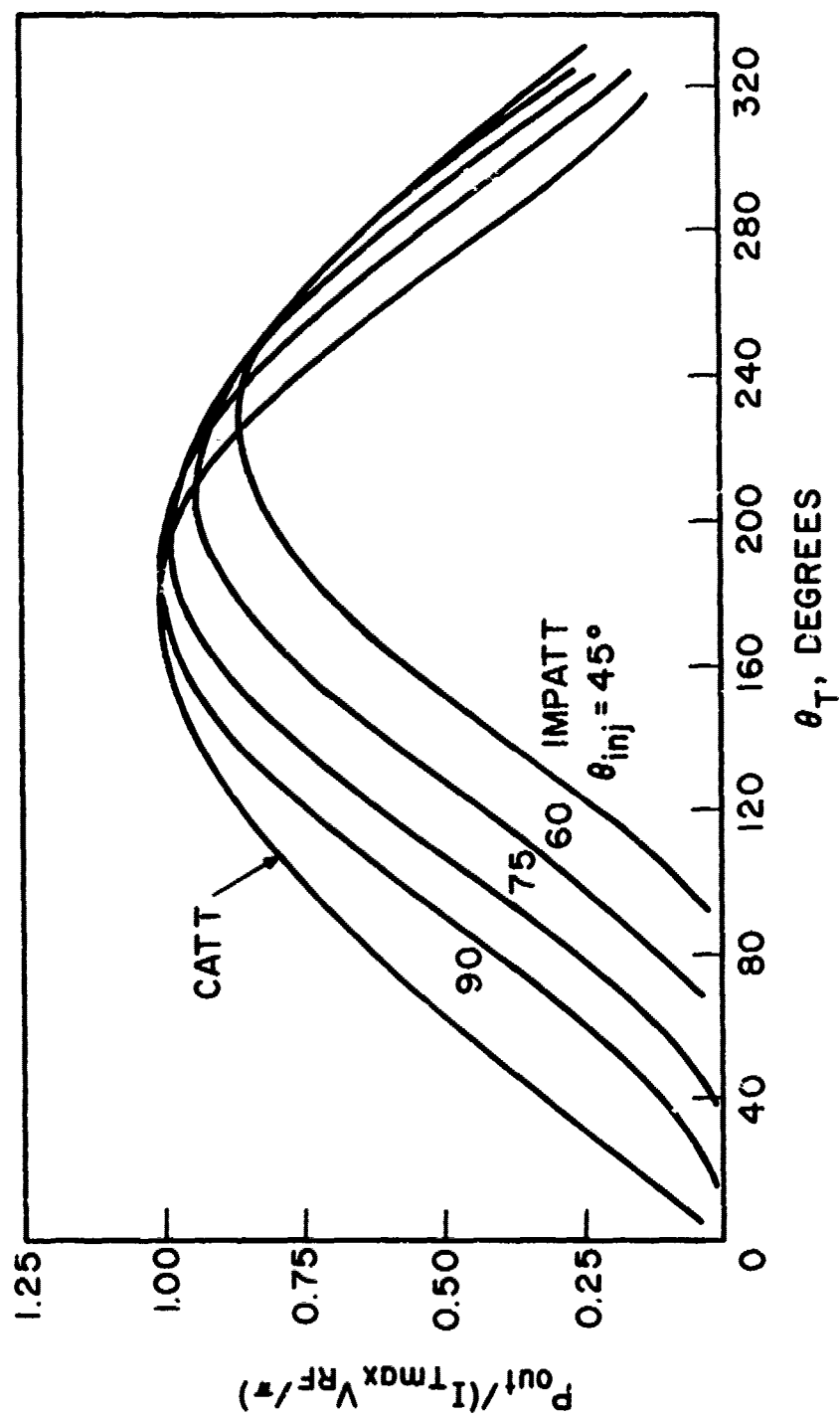
FIG. 1.5 NORMALIZED P_{out} CURVES OF CATT AND IMPATT DEVICES AT DIFFERENT θ_{inj}.

The vertical axis is labeled $P_{out}/(I_{Tmax}V_{RF}/\pi)$ with values 0, 0.25, 0.50, 0.75, 1.00, 1.25.

The horizontal axis is labeled θ_T, DEGREES with values 40, 80, 120, 160, 200, 240, 280, 320.

Curves are labeled CATT, 90, 75, 60, and IMPATT $\theta_{inj} = 45°$.
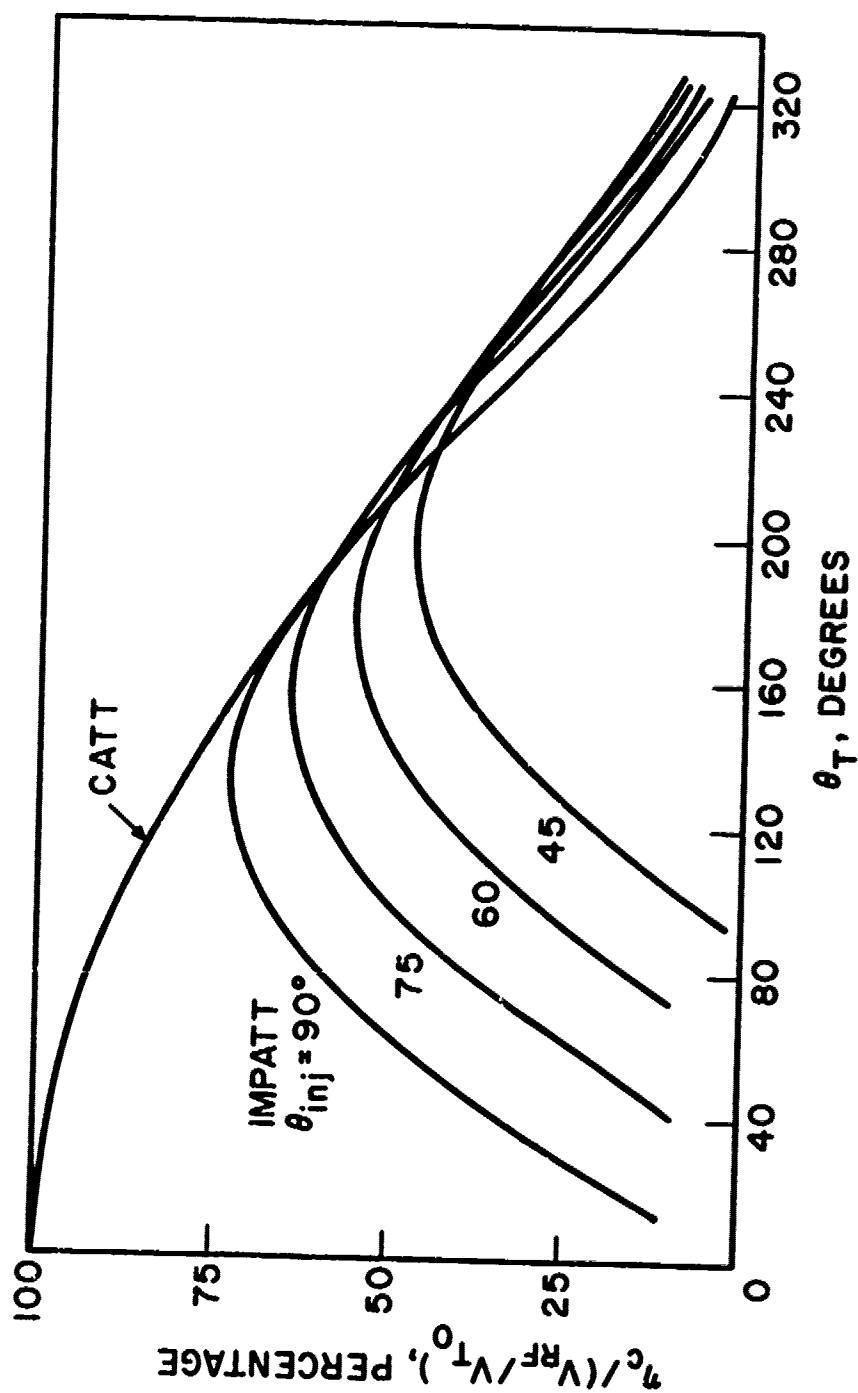
FIG. 1.6 NORMALIZED COLLECTOR EFFICIENCY CURVES OF CATT AND IMPATT DEVICES AT DIFFERENT θ_{inj}.

hand, fre▾ ·power performances are influenced through the packaging conditioi. The transistor dynamic characteristics can be seriously degraded through the package inductances and capacitances. Making external input and output matching at microwave frequencies is extremely difficult. The first attempt to eliminate this drawback was to reduce these inductances and capacitances as much as possible. Two more sophisticated solutions were developed recently. The first consists of input and output matching within the transistor packaging, the so-called chip carriers; the second does away with the package and introduces transistors directly in a microwave integrated circuit called MIC.[40,41] The first type is commercially available; the second is currently under commercial development.

The bipolar power transistors have been developed primarily for Class C applications, because in this class of operation both power and efficiency attain their highest values. However, in recent years the field of application of the BJT has been extended to Class A, with a view to reduce the nonlinearity and noise figures. The output power of the Class A BJT is also characterized by a large bandwidth and gain flatness.

Tables 1.1 and 1.2 give the electrical characteristics of BJTs for Class C amplifier and oscillator operation and the performance of Class C BJT microwave power amplifiers.[42] Similarly, Tables 1.3 and 1.4 give the electrical characteristics of BJTs in Class A amplifier and oscillator modes and the performances of Class A BJT microwave power amplifiers.[42] The results in Tables 1.1 through 1.4 represent the state of the art in 1977. More recently, a Si power BJT for use

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Table 1.1

Electrical Characteristics of Microwave Power Bipolar

Transistors (Commercially Available) for Class C

Amplifier and Oscillator Operations (Teszner and Teszner[42])

	Frequency Range (GHz) 1-4.5
Collector-base breakdown voltage, BV_{CBO} (V)	35-70
Collector-emitter breakdown voltage with shunted BE junction,[a] BV_{CER} (V)	35-60
Collector-emitter breakdown voltage (with opened BE junction), BV_{CEO} (V)	15-40
Emitter-base breakdown voltage, BV_{EBO} (V)	2-4
Collector-emitter continuous voltage, V_{CE} (V)	12-28[b]
Emitter metal finger average current density, I_{Emfa} (A cm^{-2})	~ 5 x 10^4-5 x 10^5

a. The shunting must be of sufficiently low resistance to limit the minority carrier injection as much as possible.

b. For CW operation; in pulsed-wave operation, V_{EC} is generally increased, up to 40 V.

Table 1.2

Electrical Performances of Microwave Power Bipolar

Transistors, with or Without Internal Matching,

for Class C Amplifier Operation[a] (Teszner and Teszner[42])

	Frequency Range (GHz)								
Amplifier transistor chip	1	2	4		4.2	4.5	6	8	10
Output power in CW operation,[b] P_{outmax} (W)	35	20	5	7[f]	3[d]	1[e]	1.5[g]	1.2[h]	1[h]
Amplifier power added efficiency,[c] η (percent)	60	50	30	33[f]	40[d]	25[e]	36[g]	24[h]	20[h]
Power gain PG (dB)	10	10	5	7[f]	4[d]	4[e]	4.5[g]	~5[h]	4.4[h]

a. The data given up to 4 GHz concern commercially available transistors, of both types, with or without internal matching.

b. In pulsed-wave operation, an output power level of 150 W (duty cycle ~ 1 percent) at 1 GHz with PG = 10 dB is obtained with commercially available transistors (V_{CE} being increased to 40 V).

c. The η values indicated here correspond to the P_{outmax}; however, some higher values have been obtained for lower P_{out}; in particular, at 1 GHz, η goes up to 65 percent and at 2 GHz, up to 60 percent.

d. Internally matched devices.

e. Devices without internal matching.

f. Experimental.

g. Experimental.

h. Experimental.

Table 1.3

Electrical Characteristics of Microwave Power Bipolar Transistors

(Commercially Available) for Class A Amplifier and

Oscillator Operations (Teszner and Teszner[42])

	Frequency Range (GHz) 1-4
Collector-base breakdown voltage, BV_{CBO} (V)	≥ 40
Collector-emitter breakdown voltage, BV_{CEO} (V)	≥ 15[a]
Emitter-base breakdown voltage, BV_{EBO} (V)	≥ 3
Collector-emitter continuous voltage, V_{CC} (V)	≥ 15
Collector-emitter continuous current, I_{CC} (mA)	≥ 50

---

a. For BV_{CER}, the values approximate BV_{CBO}.

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Table 1.4

Electrical Performances of Microwave Power Bipolar

Transistors, Without Internal Matching, for

Class A[a] Amplifier Operation[b] (Teszner and Teszner[42])

	Frequency Range (GHz)				
	1	2	3	4	6
Amplifier transistor chip output power in CW operation, P_{outmax} (W)	6	3	1.2	0.8	0.8
Amplifier power efficiency, η (percent)[c]	~30	~25	~20	~15	~17
Power gain PG (dB)[c]	10	10	8	6	4

----

a. A linear amplifier operating in Class B or AB with active broadband
    bias circuit has been developed in the laboratory. Compared with
    Class A amplifiers it would provide for identical I/C (intermodulation
    ratio) = ~ 20 dB, an efficiency ~ 2 times higher (15.5 vs. 8.5
    percent) with PG = 10 dB, P_{out} = 0.4 W at 4 GHz. This efficiency
    ratio seems to be increased for lower I/C; thus it becomes ~ 5 for
    I/C = ~ 30 dB, but with η decreasing to 12 and 2.2 percent,
    respectively, and proportionately P_{out}. However, all the efficiencies
    quoted remain low compared with the efficiencies of commercially
    available devices given above.

b. The data given up to 4 GHz apply to commercially available transistors.
    The data given in the last column are for an experimental model,
    under laboratory development. In both cases the output power is
    obtained at 1 dB gain compression.

c. The η and PG values correspond to P_{outmax}.

at X-band has been developed using e-beam and ion implantation.[26] The BJT has a bar size of 0.5 x 1 mm² and consists of four 27.5 x 75 µm² active cells. The combined output power of four cells operating in Class C configuration is nearly 2 W CW at 8 GHz and almost 1.5 W CW at 10 GHz.

Experimental data on Class C CATT amplifiers is very limited. The only published results are those by Yu et al.[27,33] They demonstrated the feasibility of a CATT amplifier both theoretically and experimentally from 0.5 to 4 GHz. An S-band CATT device with an emitter periphery to active base area ratio of 3.3×10^3 in^{-1} achieved a gain of 13 dB at a pulsed power output of 12 W and 28 percent power added efficiency when operated at 2 GHz. The gain at this operating point was 11 dB higher than its equivalent BJT transistor. Experimental results indicate that the impedance levels and Q values of the CATT are favorable for impedance matching, power combining and instantaneous bandwidth operation with useful gain.

1.4 Outline of the Present Study

The objective of this study is to investigate the theoretical capability of Class C CATT amplifiers and to compare them with BJT amplifiers. Analytical equations, circuit models and computer simulations are used to determine dc, small-signal, and large-signal behavior.

In Chapter II a computer program is developed which calculates the dc avalanche multiplication factor as a function of collector structure, base-collector dc bias and material parameters. Information concerning optimum collector structure for large-signal operation and suitability of various materials can be obtained.

In Chapter III analytical dc and small-signal models for CATT devices are given. Computer solutions of the analytical models are given and the results are discussed.

In Chapter IV a large-signal computer simulation is developed. The simulation calculates the RF output power and efficiency and many other parameters. Detailed descriptions of the numerical algorithms and the computer programs are given.

In Chapter V large-signal results are obtained for a series of X-band CATT and BJT devices. The computer results for both devices are given, discussed and compared.

In Chapter VI a summary of this study is given and suggestions for further work are described.

CHAPTER II.   MATERIAL PARAMETERS AND THE DC
AVALANCHE MULTIPLICATION FACTOR

2.1 Introduction

As mentioned previously, an ideal CATT device should have a dc bias point at which both a significant avalanche multiplication factor and a large RF voltage across the base-collector terminal can result. A simple computer program called AVALAN was developed which provides information on the dc avalanche multiplication factor M_{A_o} as a function of the dc base-collector terminal voltage V_{T_o}, the punch-through voltage V_{PT}, the breakdown voltage V_B, the sustaining voltage V_{sus} and the electric field (E) distribution in the collector depletion region. In this chapter the material parameters, the avalanche multiplication factor and the electric field distribution for devices of different materials and various structures are given and comparisons are made. The effects of device temperature and space charge are also described here.

2.2 Material Parameters

The material parameters required to calculate M_{A_o}, V_{PT}, V_B, V_{sus} and E are α_n, α_p, ϵ, E_{sus_n} and E_{sus_p}, where α_n and α_p are the electron and hole ionization rates, respectively, ϵ is the dielectric permittivity, and E_{sus_n} and E_{sus_p} are the electric fields required to sustain electrons and holes at their saturation velocities. These values for Si and GaAs are listed in Tables 2.1 and 2.2. Shown in Fig. 2.1 is the dc avalanche multiplication factors of two n-type Si devices, where electrons initiate the avalanche process. Figure 2.2 shows the dc avalanche multiplication factors for two p-type Si devices, where holes initiate the

Table 2.1

Material Parameters for Si $\{\epsilon = 1.04477 \times 10^{-12}$ F/cm,

$E_{sus_n} = 2 \times 10^4$ V/cm, $E_{sus_p} = 6 \times 10^4$ V/cm, $\alpha(E) =$

A exp $[- (b/E)]$ cm$^{-1}\}$

Holes		Electrons		Electric Field (kV/cm)	Reference
A_p (cm^{-1})	b_p (V/cm)	A_n (cm^{-1})	b_n (V/cm)		
T = 27°C					
2.25×10^7	3.26×10^6	3.8×10^6	1.75×10^6	200–500	Lee et al.[44]
2×10^6	1.97×10^6			200–530	Grant[43]
5.6×10^5	1.32×10^6			530–770	
		2.6×10^6	1.43×10^6	200–240	
		6.2×10^5	1.08×10^6	240–530	
		5×10^5	9.9×10^5	530–770	
T = 200°C					
1.0×10^7	3.2×10^6	1.8×10^6	1.64×10^6	200–500	Lee et al.[44]
2×10^6	2.166×10^6			200–530	Grant[43]
5.6×10^5	1.516×10^6			530–770	
		2.6×10^6	1.661×10^6	200–240	
		6.2×10^5	1.311×10^6	240–530	
		5×10^5	1.221×10^6	530–770	

Ionization Rates for Electrons and Holes

$\alpha = (1/\lambda)$ exp $[(11.5r^2 - 1.17r + 3.9 \times 10^{-4})x^2 + (46r^2$

$- 11.9r + 1.75 \times 10^{-2})x - 757r^2 + 75.5r - 1.92]$,

where $r = \langle\epsilon_r\rangle/\epsilon_i$, $x = \epsilon_i/e\lambda E$, $\epsilon_r = 0.063$ eV ,

$\langle\epsilon_r\rangle/\epsilon_r = \tanh (\epsilon_r/2kT) = \lambda/\lambda_o$,

$\epsilon_i = 1.5 \times [1.16 - 7.02 \times 10^{-4} \times T^2/(T + 1108)]$,

$\lambda_o = 76$ Å for electrons and $\lambda_o = 47$ Å for holes .

Crowell and Sze[45]

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Table 2.2

Material Parameters for GaAs ($\epsilon = 1.10675 \times 10^{-12}$ F/cm, $E_{sun_n} = 3 \times 10^3$ V/cm, $E_{sun_p} = 3 \times 10^3$ V/cm, $a(E) = A \exp[-(b/E)^n]$ cm^{-1}).

n	Holes		Electrons		Reference
	A_p (cm^{-1})	b_p (V/cm)	A_n (cm^{-1})	b_n (V/cm)	
2	$2\times10^5\times[1+(T-300)\times 7\times10^{-4}]$	$5.5\times10^5\times[1+(T-300)\times 1.2\times10^{-3}]$	$2\times10^5\times[1+(T-300)\times 7\times10^{-4}]$	$5.5\times10^5\times[1+(T-300)\times 1.2\times10^{-3}]$	Hall and Lock[46]
T = 27°C					
1	3.6×10^8	2.9×10^6	1.2×10^7	2.3×10^6	Stillman et al.[47]
T = 200°C					
2	3.15×10^5	8×10^5	3.15×10^5	8×10^5	Constant et al.[48]
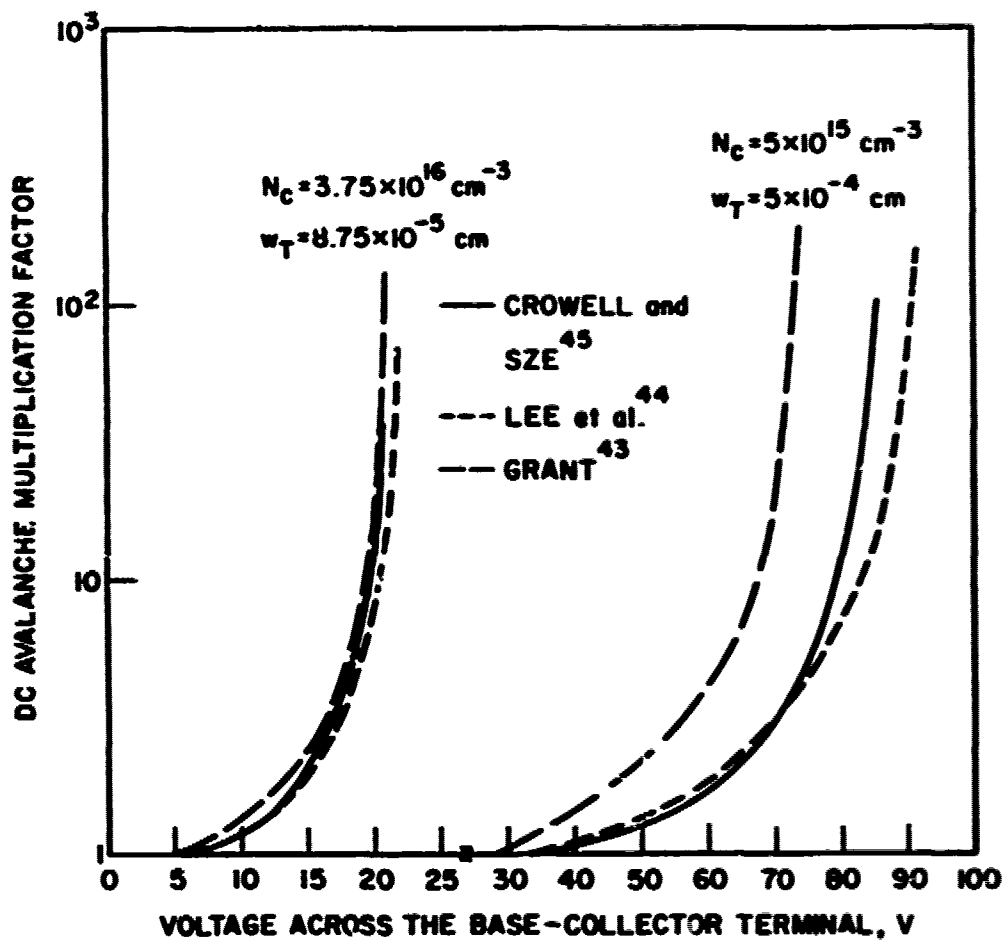
FIG. 2.1 DC AVALANCHE MULTIPLICATION FACTORS CORRESPONDING
TO VARIOUS IONIZATION RATES FOR ELECTRONS AND HOLES
AT 27°C FOR TWO n-TYPE Si COLLECTOR STRUCTURES, WHERE
ELECTRONS INITIATE THE AVALANCHE PROCESS. (UNIFORMLY
DOPED COLLECTOR STRUCTURES)
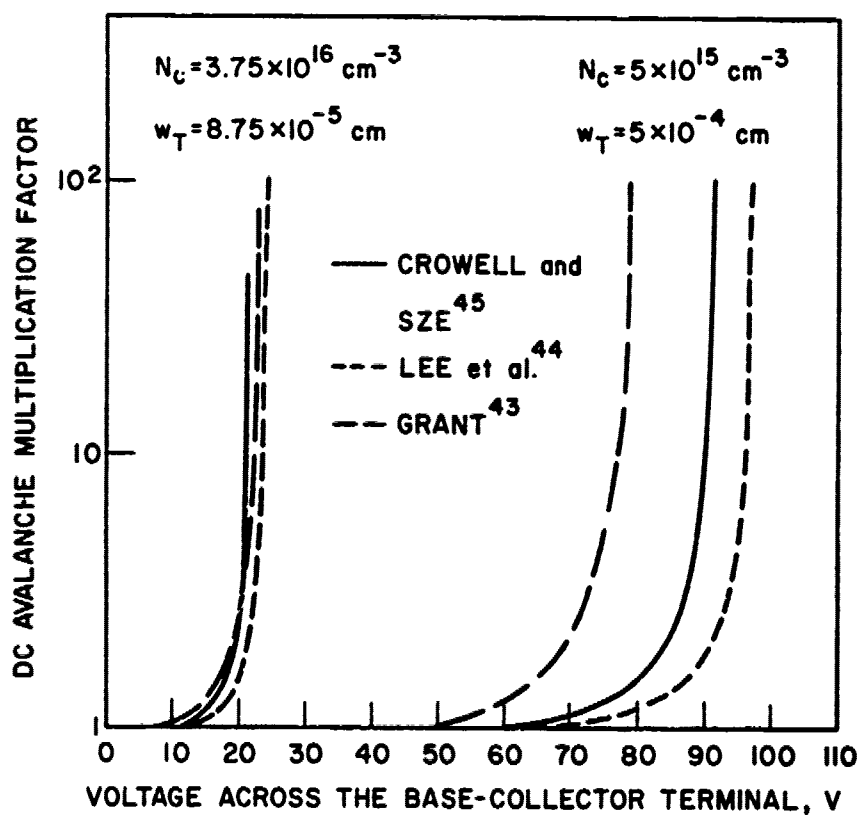
FIG. 2.2 DC AVALANCHE MULTIPLICATION FACTORS CORRESPONDING
TO VARIOUS IONIZATION RATES FOR ELECTRONS AND HOLES
AT 27°C FOR TWO p-TYPE Si COLLECTOR STRUCTURES, WHERE
HOLES INITIATE THE AVALANCHE PROCESS.   (UNIFORMLY DOPED
COLLECTOR STRUCTURES)

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avalanche process. The ionization rates of electrons and holes used
are those reported by Grant,[43] Lee et al.,[44] and Crowell and Sze.[45]
Grant's ionization rates give the lowest breakdown values. Figure 2.3
shows the dc avalanche multiplication factors of two n-type GaAs devices
where electrons initiate the avalanche process. The ionization rates
used are those obtained by Hall and Leck,[46] Stillman et al.[47] and Constant
et al.[48] The breakdown values obtained by using Hall and Leck's
ionization rates are lower. The impact avalanche ionization rates are
very important in determining the characteristics of CATT devices, but
there is some dispute about their precise values and electric field
dependence.

2.3 Dc Multiplication of Charge Carriers in n-Type and p-Type Si and n-Type GaAs CATT Devices

2.3.1 Derivation of the Analytical Expression for the Dc Avalanche Multiplication Factor of CATT Devices.

An n-type CATT device
is shown in Fig. 2.4. The electron current I_{nB} represents the electron
carriers injected into the collector depletion region, which originated
from the forward-biased emitter-base junction. While the electron
particle current is flowing in the positive x-direction, the electronic
current is positive in the negative x-direction. The dc time-independent
continuity equations for electrons and holes in the collector depletion
region are

$$\frac{dJ_n}{dx} - (\alpha_n J_n + \alpha_p J_p) = 0 \qquad (2.1)$$

and

$$\frac{dJ_p}{dx} + (\alpha_n J_n + \alpha_p J_p) = 0 \quad , \qquad (2.2)$$
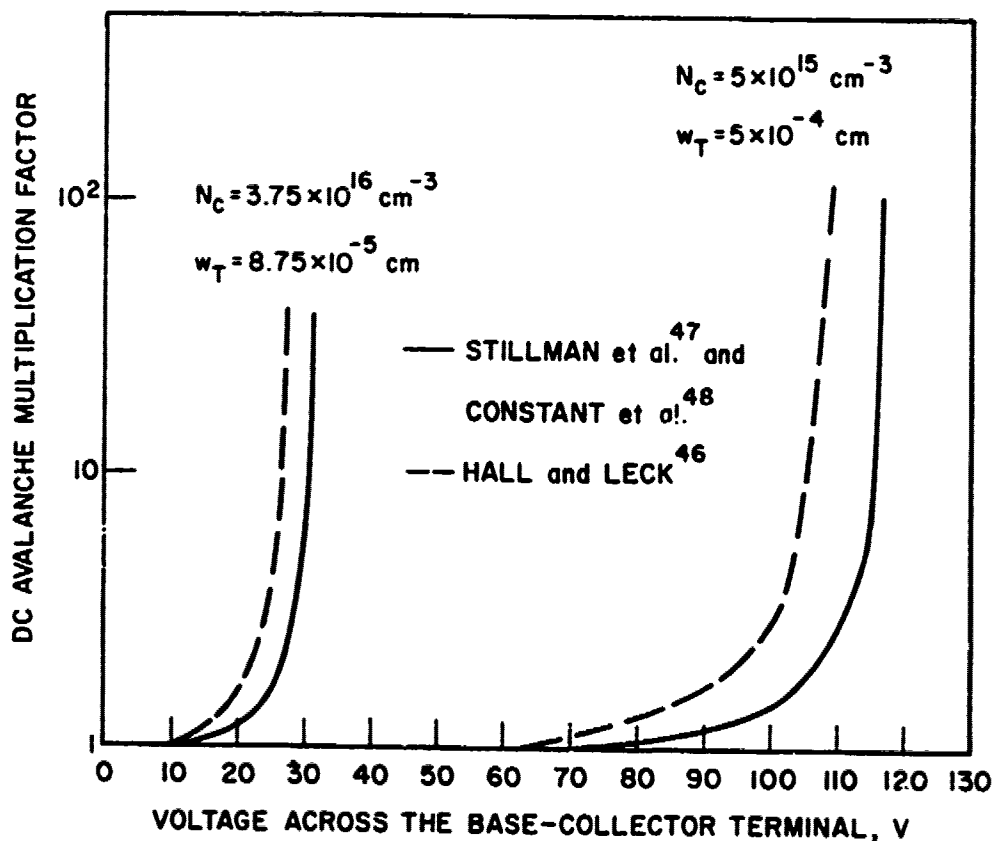
FIG. 2.3   DC AVALANCHE MULTIPLICATION FACTORS CORRESPONDING

TO VARIOUS IONIZATION RATES FOR ELECTRONS AND HOLES

AT 200°C FOR TWO n-TYPE GaAs COLLECTOR STRUCTURES,

WHERE ELECTRONS INITIATE THE AVALANCHE PROCESS.

(UNIFORMLY DOPED COLLECTOR STRUCTURES)

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| EMITTER | BASE | COLLECTOR |
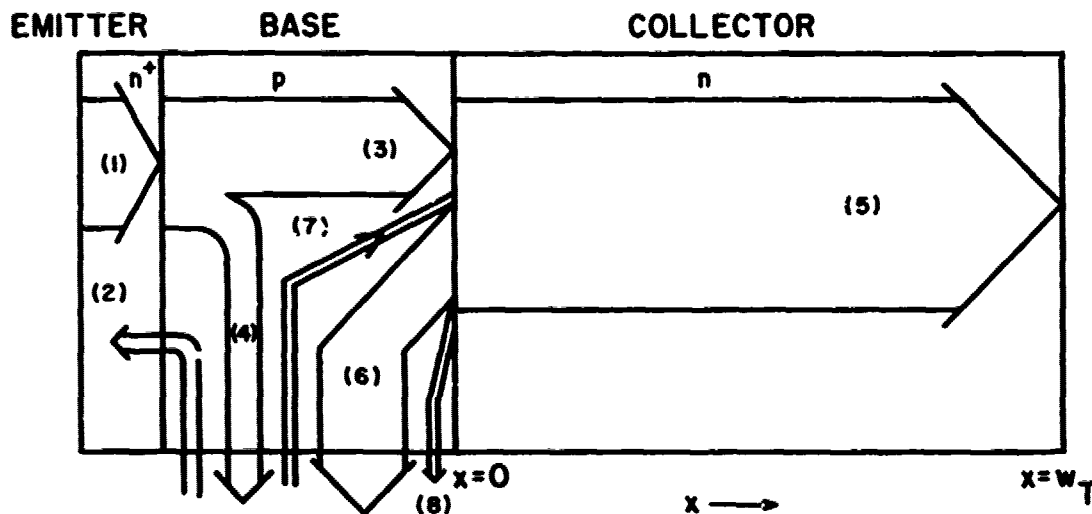
1. $- I_{nE}$, Electron Particle Current Crossing the Forward-Biased Emitter-Base Junction

2. I_{pE}, Hole Particle Current Crossing the Forward-Biased Emitter-Base Junction

3. $- I_{nB}$, Component of $- I_{nE}$ which has Reached the Base Edge of the Collector-Base Depletion Region

4. Component of $- I_{nE}$ Lost in the Base Region Due to Carrier Recombination

5. $- I_{T}$, Total Collector Particle Current

6. I_{pB}, Feedback Hole Current Due to Avalanche Multiplication

7. $- I_{c_{ns}}$, Electron Reverse Saturation Current

8. $I_{c_{ps}}$, Hole Reverse Saturation Current

FIG. 2.4   SCHEMATIC OF THE ELECTRON AND HOLE PARTICLE CURRENT

DISTRIBUTIONS IN A NORMALLY BIASED n-TYPE CATT DEVICE.

(ELECTRON PARTICLE CURRENTS HAVE OPPOSITE SENSES OF

DIRECTION TO THAT OF ELECTRONIC CURRENTS)

respectively. When Eqs. 2.1 and 2.2 are added, the result is

$$\frac{d}{dx} (J_n + J_p) = 0 \tag{2.3}$$

which indicates that the total particle current J_T is constant, independent of the space coordinate x where $J_T \overset{\Delta}{=} J_n + J_p$. The following differential equation is obtained from Eqs. 2.1 through 2.3:

$$\frac{dJ_n}{dx} + (\alpha_p - \alpha_n)J_n = \alpha_p J_T$$

whose solution is

$$J_n(x) = \frac{J_T \int_0^x \alpha_p(x') \left[\exp \int_0^{x'} [\alpha_p(x'') - \alpha_n(x'')] \, dx'' \right] dx' + c}{\exp \int_0^x [\alpha_p(x') - \alpha_n(x')] \, dx'} , \tag{2.4}$$

where the constant c is determined by imposing the proper boundary conditions. The boundary conditions are

$$J_n(0) = J_{c_{ns}} + J_{nB}$$

and

$$J_p(w_T) = J_{c_{ps}} ,$$

where $J_{c_{ns}}$ and $J_{c_{ps}}$ are the collector reverse saturation currents. By using Eqs. 2.3 and 2.4 and the boundary conditions, the following expression can be obtained:

$$J_T = \frac{J_{c_{ps}} \exp \int_0^{W_T} (\alpha_p - \alpha_n) \, dx + J_{nB} + J_{c_{ns}}}{\exp \int_0^{W_T} (\alpha_p - \alpha_n) dx - \int_0^{W_T} \alpha_p \left(\exp \int_0^x [\alpha_p(x') - \alpha_n(x')] \, dx' \right) dx} \quad ,$$

which can be further reduced to

$$J_T = \frac{J_{c_{ps}} \exp \int_0^{W_T} (\alpha_p - \alpha_n) \, dx + J_{nB} + J_{c_{ns}}}{1 - \int_0^{W_T} \alpha_n \left(\exp \int_0^x [\alpha_p(x') - \alpha_n(x')] dx' \right) dx} \qquad (2.5)$$

by using the relation

$$\frac{d}{dx} \exp \int_0^x f(x') \, dx' = \left(\exp \int_0^x f(x') \, dx' \right) [f(x)] \quad .$$

When the emitter-base junction is forward biased, the relation

$$J_{nB} \gg J_{c_{ps}} \exp \int_0^{W_T} (\alpha_p - \alpha_n) \, dx$$

is true for any base-collector reverse bias voltage up to a value signif-icantly above the breakdown value. Therefore, Eq. 2.5 can be reduced to

$$J_T \simeq M_{A_o} (J_{nB} + J_{c_{ns}}) \quad , \qquad (2.6)$$

where the dc avalanche multiplication factor is given by

$$M_{A_o} = \frac{1}{1 - \int_0^{w_T} \alpha_n \left(\exp \int_0^x [\alpha_p(x') - \alpha_n(x')]dx' \right) dx} . \qquad (2.7)$$

The expression in Eq. 2.7 is used to calculate the carrier multiplication and the breakdown voltage when the avalanche process is initiated by electrons as in n-type CATT devices.

For p-type CATT devices, where the avalanche process is initiated by holes, expressions for J_T and M_{A_o} can be similarly derived and they are

$$J_T = M_{A_o}(J_{pB} + J_{c_{ps}}) \qquad (2.8)$$

and

$$M_{A_o} = \frac{1}{1 - \int_0^{w_T} \alpha_p \left(\exp \int_0^x [\alpha_n(x') - \alpha_p(x')] dx' \right) dx} . \qquad (2.9)$$

2.3.2 Dc Avalanche Multiplication Factor vs. V_T Characteristics in n-Type and p-Type Si and n-Type GaAs CATT Devices. A distinction can be made on the dc avalanche multiplication factor vs. the base-collector terminal voltage characteristic which depends on the amount of feedback in the avalanche process. This distinction is made clear by investigating three cases of n-type Si CATT devices. The first one is for the case where the ionization coefficients α_n and α_p are assigned realistic values. The second one is where the hole ionization

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coefficient α_p is assigned to be equal to the electron ionization coefficient α_n, and the third one is where the hole ionization coefficient α_p is set to zero. In p-type Si CATT devices, the second and third cases are when α_n is assigned to be equal to α_p and when α_n is set to zero, respectively. For n-type devices, where in reality $\alpha_n > \alpha_p$, the second case represents a situation where the positive feedback in the avalanche process is artificially increased, and the dc avalanche multiplication rises more rapidly with increasing bias voltage. In this case, to achieve significant carrier multiplication, the bias voltage must be set very close to the breakdown value which, on the other hand, would severely limit the allowed RF voltage amplitude V_{RF}. For p-type Si devices, the second case represents a situation where the positive feedback in the avalanche process is artificially reduced since $\alpha_p < \alpha_n$ in reality and M_{A_o} rises slower with increasing bias voltage. The third case represents a situation, for both n-type and p-type devices, where there is no positive feedback in the avalanche process, and multiplication occurs during a single transit of the high field region. The multiplication factor M_{A_o} rises slowest in the third case in which, theoretically, the breakdown voltage is infinite. The various cases described previously are depicted in Figs. 2.5 and 2.6.

When the realistic ionization coefficients formulated by Crowell and Sze are used for Si and those by Hall and Leck are used for GaAs, M_{A_o} vs. V_T characteristics of several CATT devices whose collector regions are uniformly doped at various impurity levels are displayed in Figs. 2.7 through 2.9. The width of the collector regions
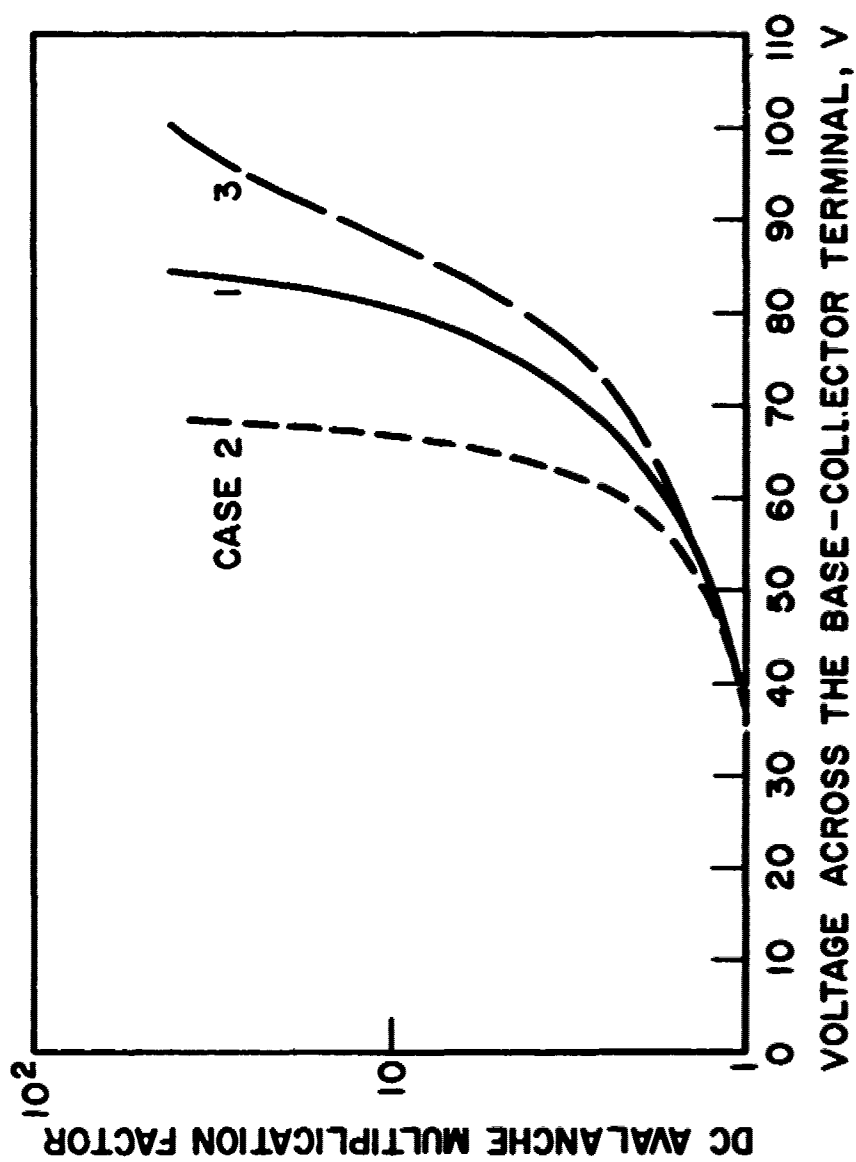
FIG. 2.5 CALCULATED M_{A_o} VS. V_T IN AN n-TYPE Si CATT DEVICE. ($w_T = 5 \times 10^{-4}$ cm, $N_c = 5 \times 10^{15}$ cm^{-3} AND $T = 27^{\circ}$C)
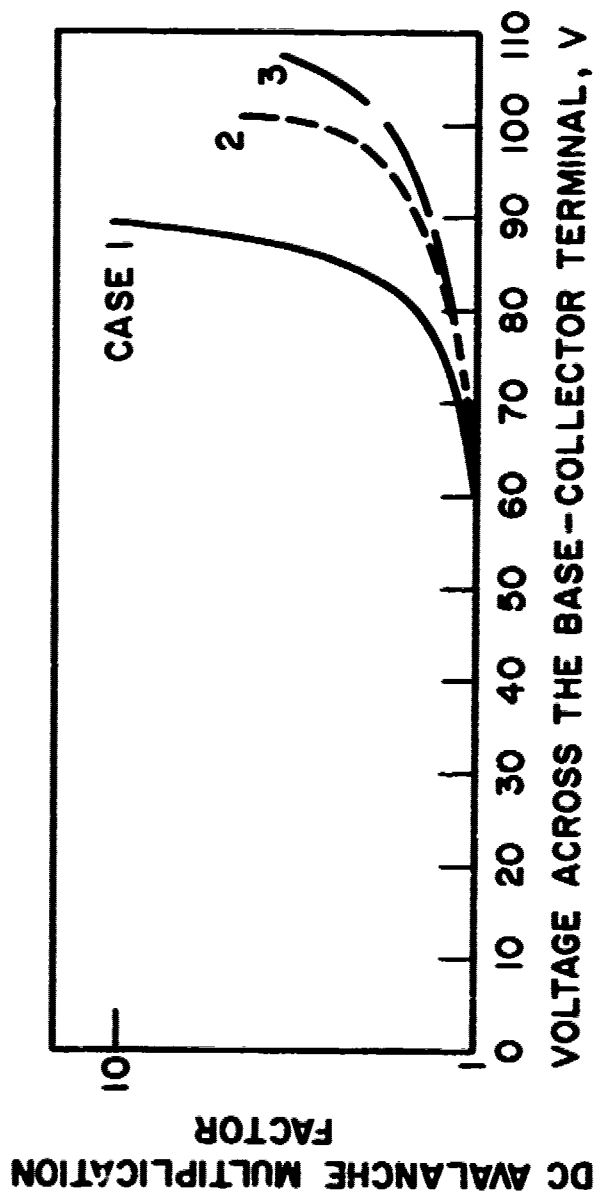
FIG. 2.6 CALCULATED M_{A_0} VS. V_T IN A p-TYPE Si CATT DEVICE. ($v_T = 5 \times 10^{15}$ cm, $N_c = 5 \times 10^{15}$ cm^{-3} AND T = 27°C)
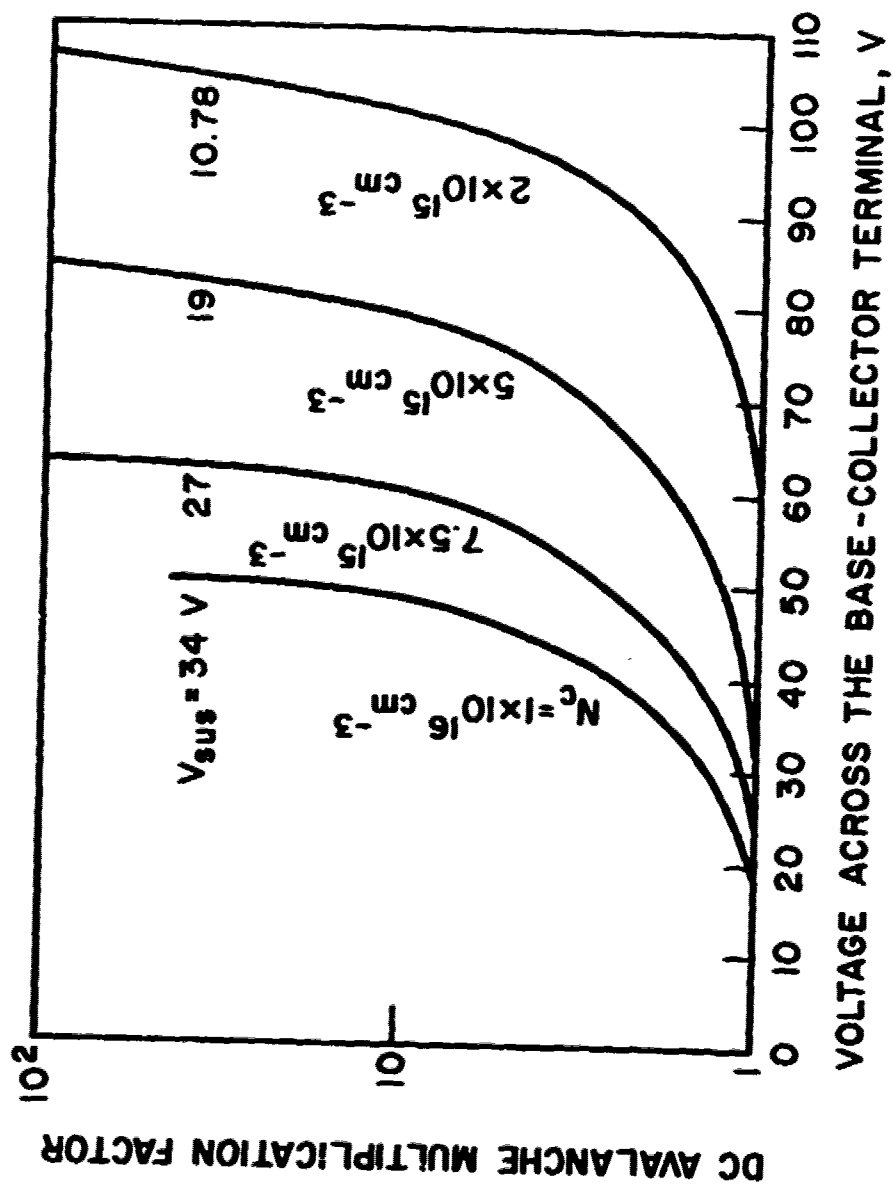
FIG. 2.7 M_{A_0} VS. V_T CHARACTERISTICS OF n-TYPE Si CATT DEVICES WHOSE COLLECTOR REGIONS ARE UNIFORMLY DOPED. ($w_T = 4 \times 10^{-4}$ cm AND T = 27°C)
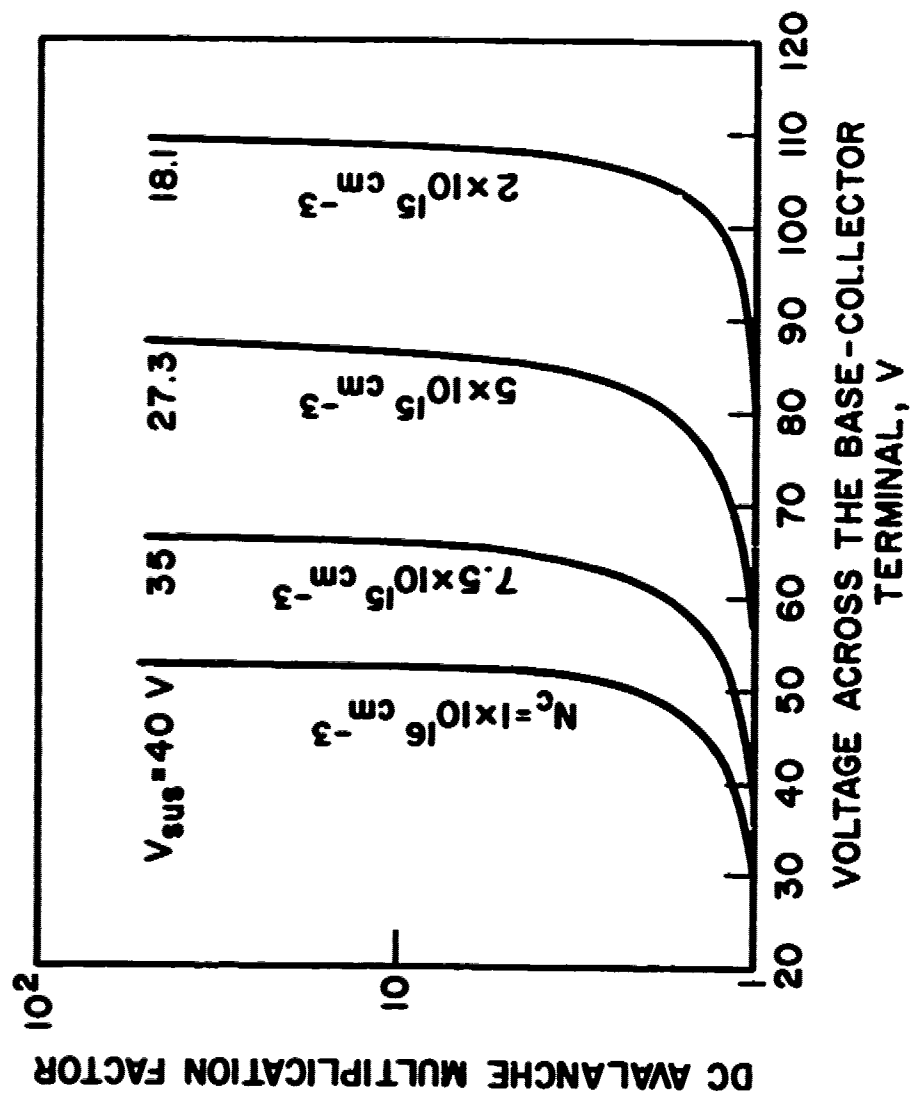
FIG. 2.8 M_{A_o} VS. V_T CHARACTERISTICS OF p-TYPE Si CATT DEVICES WHOSE COLLECTOR REGIONS ARE UNIFORMLY DOPED. ($w_T = 4 \times 10^{-4}$ cm AND $T = 27°C$)
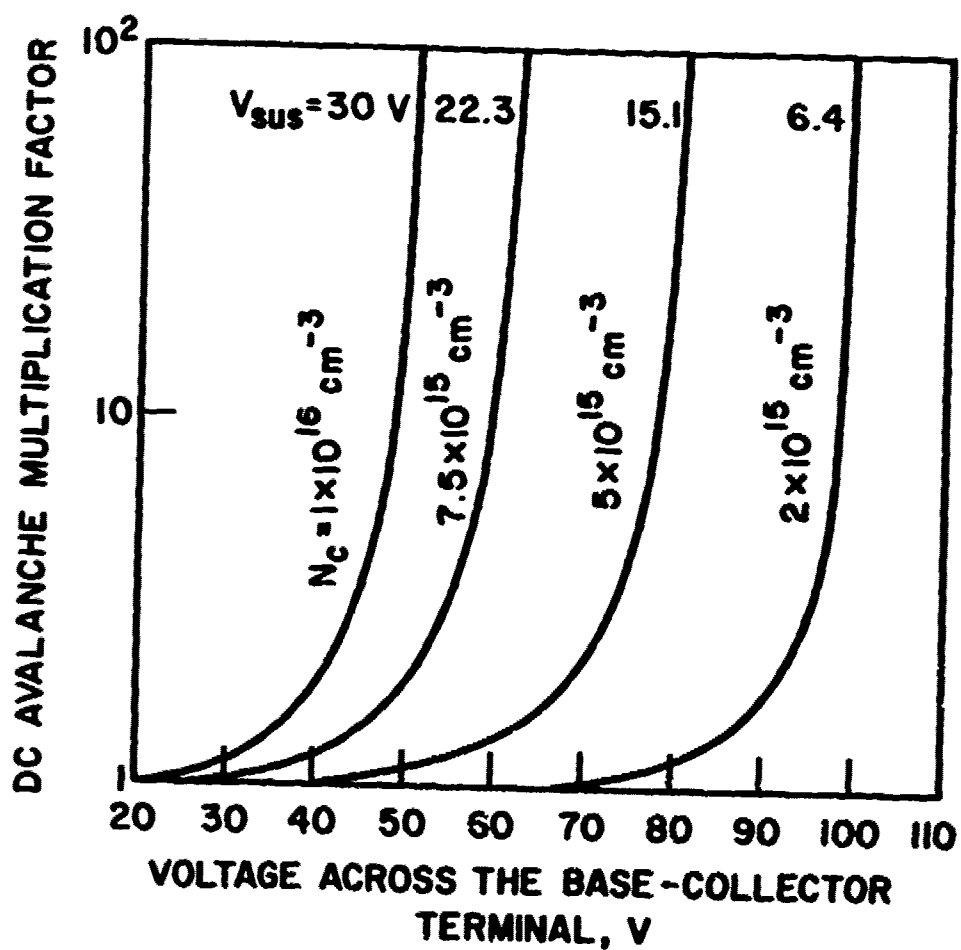
FIG. 2.9 M_{A_o} VS. V_T CHARACTERISTICS OF n-TYPE GaAs CATT DEVICES WHOSE COLLECTOR REGIONS ARE UNIFORMLY DOPED. (w_T = 4×10^{-4} cm AND $T = 27°C$)

in all cases is 4×10^{-4} cm and the CATT devices in Figs. 2.7 through 2.7 are at 27°C. The breakdown voltage of each device can be approximately defined to be the V_T value at which M_{A_o} reaches 100. The optimum load for a Class C CATT amplifier is a high-Q tank circuit whose resonant frequency is tuned at the signal frequency. Injection of a sharp pulse of charge which traverses across the depleted collector region would result in an induced current waveform and an RF voltage V_T waveform as shown in Fig. 2.10. It is observed that at $\theta = 270$ degrees, V_T is minimum and the sharp pulse of charge is located spatially near the midpoint of the collector region. An estimation of the allowed minimum V_T of a uniformly doped collector structure is V_{sus} by definition and its value[*] is

$$V_{sus} = \frac{1}{2} w_{V_{sus}} E(0) \quad , \tag{2.10}$$

where

$$w_{V_{sus}} = E(0)/(eN_c/\epsilon)$$

and

$$E(0) = \frac{1}{2} w_T \frac{eN_c}{\epsilon} + E_{sus} \quad .$$

The electric field profile at $\theta = 270$ degrees and when V_T equals the minimum allowed value V_{sus} is shown in Fig. 2.10. The value of V_{sus}

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[*] For HI-LO collector structures, the appropriate expressions for calculating V_{sus} are given in Section 2.3.3.
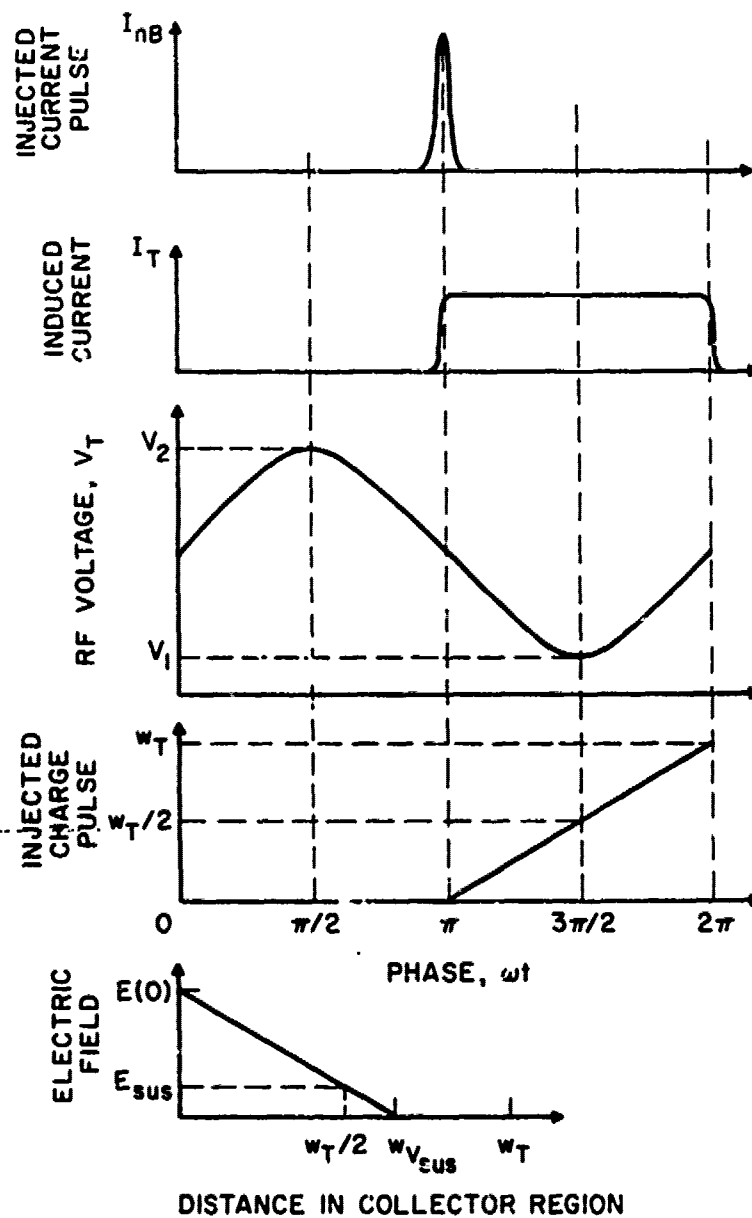
FIG. 2.10 INJECTED CURRENT, INDUCED CURRENT, TERMINAL VOLTAGE

AND POSITION OF INJECTED CHARGE PULSE VS. PHASE, AND

ELECTRIC FIELD PROFILE AT PHASE = $3\pi/2$ AND WHEN V_T =

V_{sus} IN A UNIFORMLY DOPED COLLECTOR REGION.

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for each device is also indicated in Figs. 2.7 through 2.9. Voltages V_B and V_{sus} roughly represent the upper and lower limits on V_T. It is clear from the M_{A_o} vs. V_T characteristics that n-type CATT devices are more suitable for making high gain Class C amplifiers. For p-type Si devices, although their breakdown values are slightly higher than those of similarly structured n-type Si devices, their dc bias must be set much closer to the breakdown value in order to achieve significant carrier multiplication which severely reduces the allowed amplitude of V_T. Another disadvantage of p-type devices is their higher V_{sus} which again would limit the RF voltage amplitude. For n-type GaAs devices, although their V_{sus} are slightly lower than those of similarly structured n-type Si devices, their M_{A_c} vs. V_T characteristics are such that the dc bias must be set closer to the breakdown values.

Because of its favorable M_{A_o} vs. V_T characteristic and the advanced Si technology, the investigation of Class C CATT amplifiers was concentrated mainly on n-type Si devices. It should be noted that thus far space-charge effects were ignored in determining the M_{A_o} vs. V_T characteristic, V_B, V_{sus} and electric field profile. These effects will be examined briefly in Section 2.3.4. It should also be mentioned that the V_B determined from the M_{A_o} vs. V_T characteristic is higher than the actual V_B because the effect of the base-collector junction curvature[49,50] on V_B is ignored.

2.3.3 Effects of Collector Structure on M_{A_o} vs. V_T Characteristic of n-Type Si CATT Devices. In this section, the effects of changing the doping density N_{av} in the high doping region of HI-LO

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collector structures, the effect of changing the doping density N_{drift} in the drift region, and the effects of changing the length w_D of the drift region on the dc M_{A_o} vs. V_T characteristic, V_B and V_{sus} are studied. In actual large-signal operation, V_T can be significantly higher than V_B and slightly lower than V_{sus}, but the voltages V_B and V_{sus} can serve as a guide for the upper and lower limits of V_T. The large-signal power gain, to the first-order approximation, is proportional to the product of M_{A_o} and V_{RF}, where V_{RF} is the amplitude of the RF base-collector terminal voltage, and its value is dependent on both the M_{A_o} vs. V_T characteristic and the base-collector dc bias. The dc bias is chosen to maximize the product of M_{A_o} and V_{RF} but it must not be lower than V_{PT} in order to avoid large collector resistance due to the undepleted high-resistivity collector region.

V_{sus}, the minimum V_T allowed, for HI-LO collector structures is given by

$$V_{sus} = \frac{1}{2}\left\{ [E(0) + E(w_{av})] \times w_{av} + \frac{1}{2} E(w_{av}) \times w_{V_{sus}} \right\} , \qquad (2.11)$$

where

$$E(w_{av}) = \frac{eN_{drift}}{\varepsilon} \times \left(\frac{w_T}{2} - w_{av}\right) + E_{sus} ,$$

$$E(0) = \frac{eN_{av}}{\varepsilon} \times w_{av} + E(w_{av})$$

and

$$w_{V_{sus}} = E(w_{av}) \times \varepsilon/(eN_{drift}) .$$

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The doping profile and the electric field profile at a phase angle =
$3\pi/2$ and $V_T = V_{sus}$ are shown in Fig. 2.11.

The space-charge effect and the effect of the base-collector
junction curvature are ignored. All devices are operated at 270°C.

2.3.3a Effects of Different Doping Densities N_{av}. It

can be seen from Fig. 2.12 and the data in Table 2.3 that V_{RF} varies
with V_{bias}, the base-collector dc bias. At optimum V_{bias}, devices with
higher N_{av} have lower V_{RF}, but M_{A_o} is higher for devices with higher
N_{av}. The device with $N_{av} = 2 \times 10^{16}$ cm^{-3} appears to be most suitable
for making a high RF power gain amplifier since it has the highest
$M_{A_o} - V_{RF}$ product. Moreover, the optimum dc bias is lower for devices
with higher N_{av} which means lower dc power dissipation in the collector
region at equal dc collector current densities. When N_{av} equals
3×10^{16} cm^{-3} or higher, V_{PT} is even higher than V_B.

When the space-charge effect is incorporated into the analysis,
as is done in Section 2.3.4, M_{A_o} decreases significantly with increas-
ing dc collector current density while V_B and V_{RF} increase. There-
fore, the optimum V_{bias} and N_{av} will be different from the values
extracted from Fig. 2.12.

2.3.3b Effects of Different Doping Densities N_{drift}.

From Fig. 2.13 and Table 2.4, it is clear that devices with higher
N_{drift} have higher V_{PT} and V_{sus} and lower V_B. Therefore, higher N_{drift}
implies lower V_{RF}. From the data in Table 2.4, the optimum V_{bias} for
a device with $N_{drift} = 5 \times 10^{14}$ cm^{-3} appears to be only slightly below
V_B. At $V_{bias} = 65$ V, V_{RF} is only 2 V but M_{A_o} is approximately 60 and
the $M_{A_o} - V_{RF}$ product is higher than that corresponding to lower V_{bias}.

DOPING PROFILE

ELECTRIC FIELD PROFILE
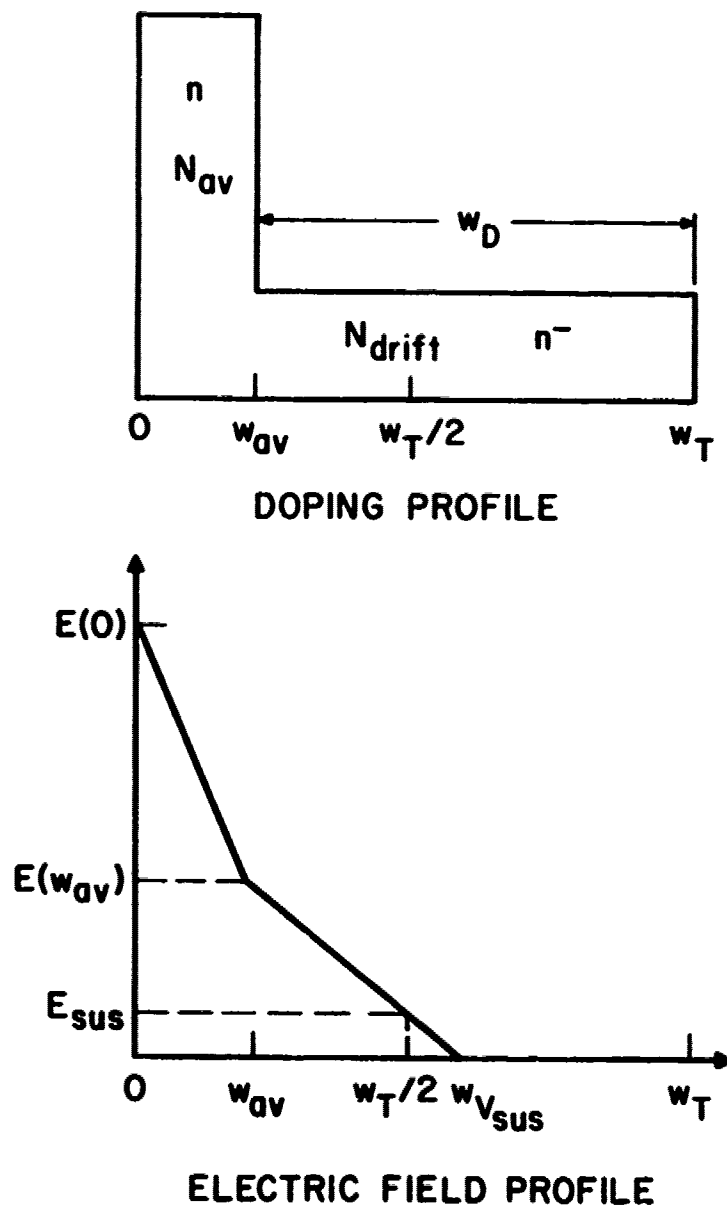
FIG. 2.11 DOPING PROFILE OF A HI–LO COLLECTOR REGION AND

THE ELECTRIC FIELD PROFILE AT A PHASE ANGLE $= 3\pi/2$

AND WHEN $V_T = V_{sus}$.
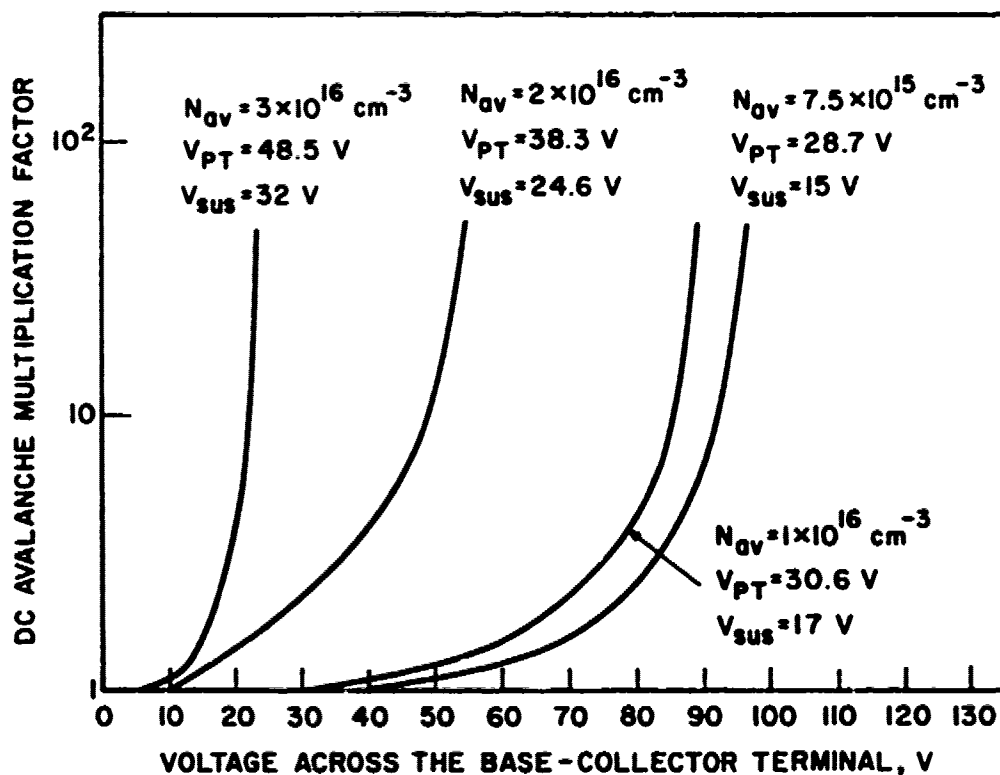
FIG. 2.12 DEPENDENCE OF M_{A_o} VS. V_T CHARACTERISTIC ON

N_{av}. (n-TYPE, Si, w_{av} = 1 x 10^{-4} cm, N_{drift} =

2 x 10^{15} cm^{-3}, w_D = 3 x 10^{-4} cm AND T = 23°C)

Table 2.3

V_{RF} and M_{A_o} at Different Dc Biases (Extracted from Fig. 2.12)

Devices: n-Type, Si, $w_{av} = 1 \times 10^{-4}$ cm, $N_{drift} = 2 \times 10^{15}$ cm^{-3}, $w_D = 3 \times 10^{-4}$ cm, T = 27°C and Different N_{av}

$N_{av} = 7.5 \times 10^{15}$ cm^{-3}

V_{bias} (V)	V_{RF} (V)	M_{A_o}	$M_{A_o} \times V_{RF}$
28.7	13.7	1.0	13.7
50	35	1.1	38.5
55	40	1.15	46
60	36	1.23	44.3
70	26	1.59	41.3
80	16	2.45	39.3
90	6	6.2	37.2

$N_{av} = 1 \times 10^{16}$ cm^{-3}

30.6	13.6	1.01	13.7
40	23	1.09	25.1
50	33	1.23	40.6
55	35	1.35	47.3
60	30	1.5	45
70	20	2.2	44
85	5	8.4	42

(Cont.)

Table 2.3 (Cont.)

$N_{av} = 2 \times 10^{16} \; cm^{-3}$

38.3	13.7	3.45	47.3
40	15.4	3.9	60.1
42.5	12.5	4.75	59.3
45	10	6	60
50	5	12	60
52.5	2.5	21	52.5
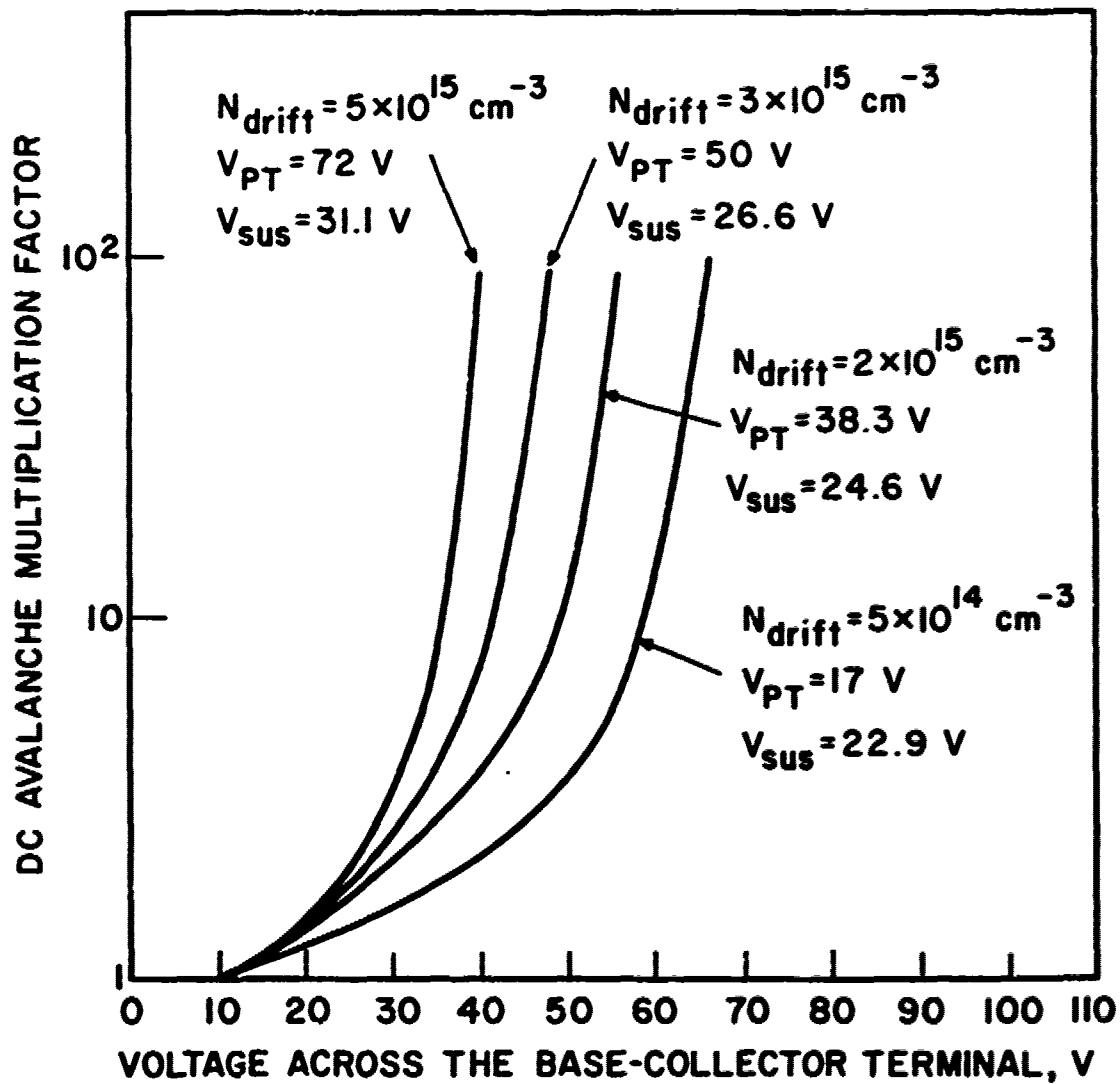
FIG. 2.13 DEPENDENCE OF M_{A_o} VS. V_T CHARACTERISTIC ON N_{drift}. (n-TYPE, Si, $N_{av} = 2 \times 10^{16}$ cm^{-3}, $w_{av} = 1 \times 10^{-4}$ cm, $w_D = 3 \times 10^{-4}$ cm AND $T = 23^\circ$C)

Table 2.4

Data V_{RF} and M_{A_o} at Different Dc Biases (Extracted from Fig. 2.13)

Devices: n-Type, Si, $N_{av} = 2 \times 10^{16}$ cm^{-3}, $w_{av} = 1 \times 10^{-4}$ cm,
$w_D = 3 \times 10^{-4}$ cm, T = 27°C and Different N_{drift}

$N_{drift} = 5 \times 10^{14}$ cm^{-3}

V_{bias} (v)	V_{RF} (v)	M_{A_o}	$M_{A_o} \times V_{RF}$
22.9	0	1.35	0
25	2.1	1.4	2.94
30	7.1	1.58	11.2
40	17.1	2.2	37.6
45	22.1	2.8	61.9
50	17	3.7	62.9
55	12	5.6	67.2
60	7	13.6	91
65	2	60	120

$N_{drift} = 2 \times 10^{15}$ cm^{-3}

38.3	13.7	3.45	47.3
40	15.4	3.9	60.1
42.5	12.5	4.75	59.3
45	10	6	60
50	5.5	12	66
52.5	3.5	21	73.5

In real situations, the space-charge effect drastically reduces M_{A_o} at high V_{bias} values and the optimum V_{bias} is significantly below V_B. From the data in Table 2.4, it appears that the lower N_{drift} the better. This is true in real situations only if the space-charge density does not exceed the collector impurity level significantly. Otherwise, the spatial direction of increasing electric field reverses.

2.3.3c Effects of Different Drift Region Widths. The effects of increasing the drift region width can be seen from the M_{A_o} vs. V_T characteristic in Fig. 2.14 and the data in Table 2.5. Longer collectors have higher breakdown values, but V_{PT} and V_{sus} are also higher. A device with $w_D = 7.5 \times 10^{-4}$ cm has the largest V_{RF}. Although the device with $w_D = 1 \times 10^{-3}$ cm has the smallest V_{RF} because of its much larger M_{A_o}, it has the highest $M_{A_o}-V_{RF}$ product. The aforementioned space-charge effect will change this result. The drift region width which corresponds to the highest $M_{A_o}-V_{RF}$ product in real situations is shorter than 1×10^{-3} cm. In actual large-signal operation, the carrier multiplication factor is not only dependent on V_{bias} but is also dependent on V_{RF} and the injection angle θ_{inj} which is dependent on ω and w_D. The amplifier efficiency, maximum RF power output and RF power gain cannot be understood in terms of V_{bias}, M_{A_o} and V_{RF} alone. The large-signal operation of Class C CATT amplifiers is discussed in detail in Chapters IV and V.

2.3.4 Temperature and Space-Charge Effects in n-Type Si CATT Devices. The effect of device temperature[45,48] can be seen from Fig. 2.15. The ionization rates of electrons and holes decrease with increasing temperature and therefore the breakdown voltage increases with increasing temperature.
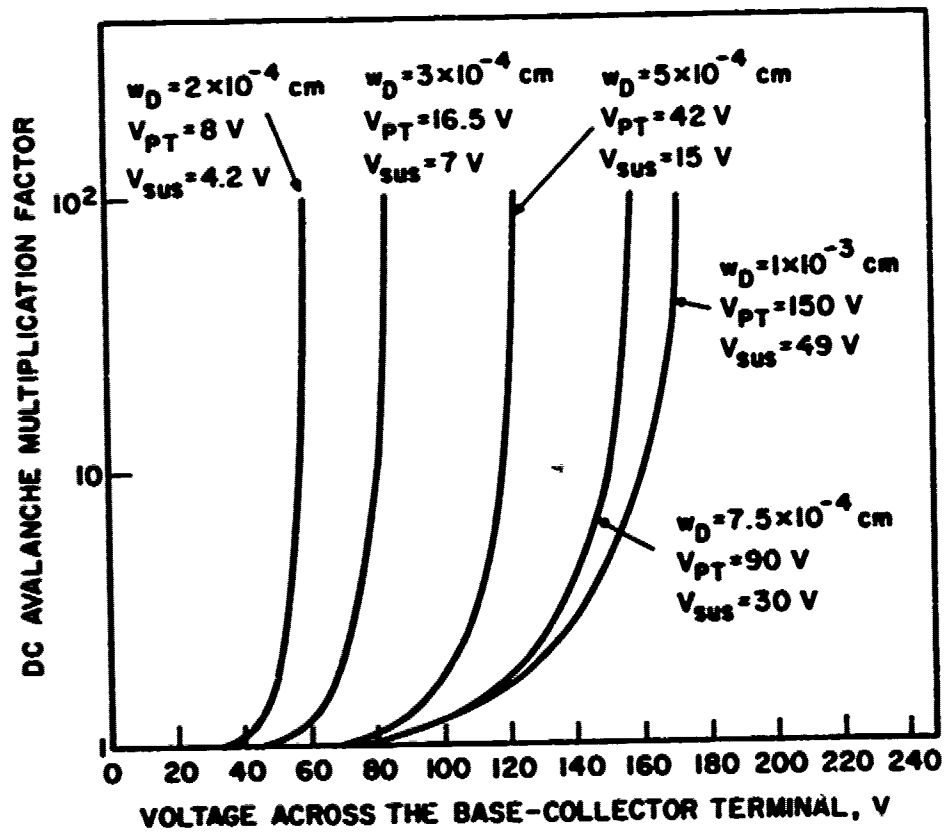
FIG. 2.14 DEPENDENCE OF M_{A_o} VS. V_T CHARACTERISTIC ON w_D. (n-TYPE, Si, UNIFORMLY DOPED COLLECTOR REGION, $N_c = 2 \times 10^{15}$ cm^{-3} AND T = 23°C)

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Table 2.5

V_{RF} and M_{A_o} at Different Dc Biases (Extracted from Fig. 2.14)

Devices: n-Type, Si, Uniformly Doped Collector, $N_c = 2 \times 10^{15}$ cm^{-3}, T = 27°C and Different w_D

$w_D = 2 \times 10^{-4}$ cm

V_{bias} (V)	V_{RF} (V)	M_{A_o}	$M_{A_o} \times V_{RF}$
8	3.8	1.0	3.8
25	20.8	1.0	20.8
30	25.8	1.0	25.8
35	25	1.01	25.3
40	20	1.1	22
50	10	2	20
55	5	4	20

$w_D = 3 \times 10^{-4}$ cm

16.5	9.5	1.0	9.5
40	33	1.0	33
45	38	1.0	38
50	34	1.05	35.7
60	24	1.25	30
70	14	2.1	29.4
80	4	7.8	31.2

(Cont.)

Table 2.5 (Cont.)

$w_D = 5 \times 10^{-4}$ cm

42	27	1.0	27
60	45	1.0	45
65	50	1.0	50
70	52	1.0	52
80	42	1.12	47
95	27	1.5	40.5
110	12	3.2	38.4
120	2	15	30

$w_D = 7.5 \times 10^{-4}$ cm

90	60	1.12	67.2
95	61	1.17	71.4
100	56	1.23	68.9
120	36	1.8	64.8
140	16	4.25	68
150	6	10	60

$w_D = 1 \times 10^{-3}$ cm

150	20	5	100
155	15	6.1	91.5
160	10	10	100
165	5	16	80
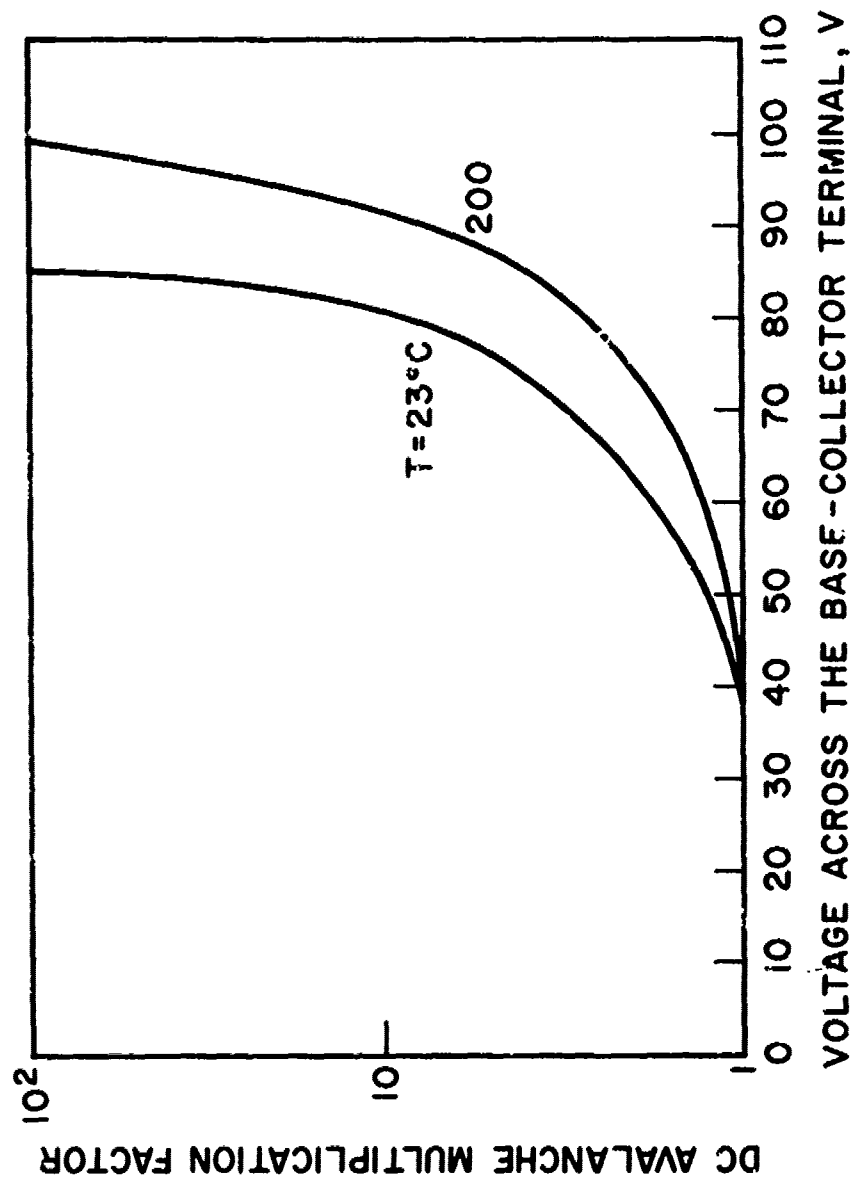
FIG. 2.15 DEPENDENCE OF M_{A_0} VS. V_T CHARACTERISTIC ON TEMPERATURE. (n-TYPE, Si, UNIFORMLY DOPED COLLECTOR AND $w_T = 5 \times 10^{-4}$ cm)

The effect of space charge[9,51] on M_{A_0} can be seen from Fig. 2.16. The upper limit on dc collector current density is dependent on N_{av} and N_{drift}. The electric field profile in a typical HI-LO collector is depicted in Fig. 2.17. As $J_{T_{dc}}$ increases while V_T is held constant, $E(w_{av})$ decreases. If the space-charge density is higher than N_{drift}, $E(w_T)$ is higher than $E(w_{av})$. If N_{av} is very high, $E(w_{av})$ at $J_{T_{dc}} = 0$ is low and it does not take a space-charge density much higher than N_{drift} to force $E(w_{av})$ below E_{sus}. If N_{drift} is very low, the electric field in the region $0 \lesssim x \lesssim w_{av}$ decreases rapidly with increasing $J_{T_{dc}}$ while V_T is held constant, therefore, M_{A_0} decreases rapidly with increasing $J_{T_{dc}}$. Moreover, the sign of dE/dx is reversed at lower $J_{T_{dc}}$ which means that $E(w_T)$ is higher than $E(w_{av})$. The condition that no significant carrier multiplication occurs near $x = w_T$ is violated at lower $J_{T_{dc}}$ for devices with lower N_{drift}. A situation could arise where the collector region near $x = 0$ becomes undepleted before $E(w_T)$ is sufficiently high to cause significant carrier generation. This collector current induced neutral region will effectively increase the effective neutral base region width and the base transport factor will decrease. This case is shown in Fig. 2.17 and corresponds to $J_{dc} = J_x$. The aforementioned space-charge effects have been demonstrated by applying AVALAN on various collector structures at different dc collector current densities.

2.4 Summary

This chapter contained the ionization rates of electrons and holes in Si and GaAs and comparisons of the dc avalanche multiplication factor vs. V_T characteristics of n-type and p-type Si and n-type GaAs CATT devices. n-type Si devices are found to have the most suitable

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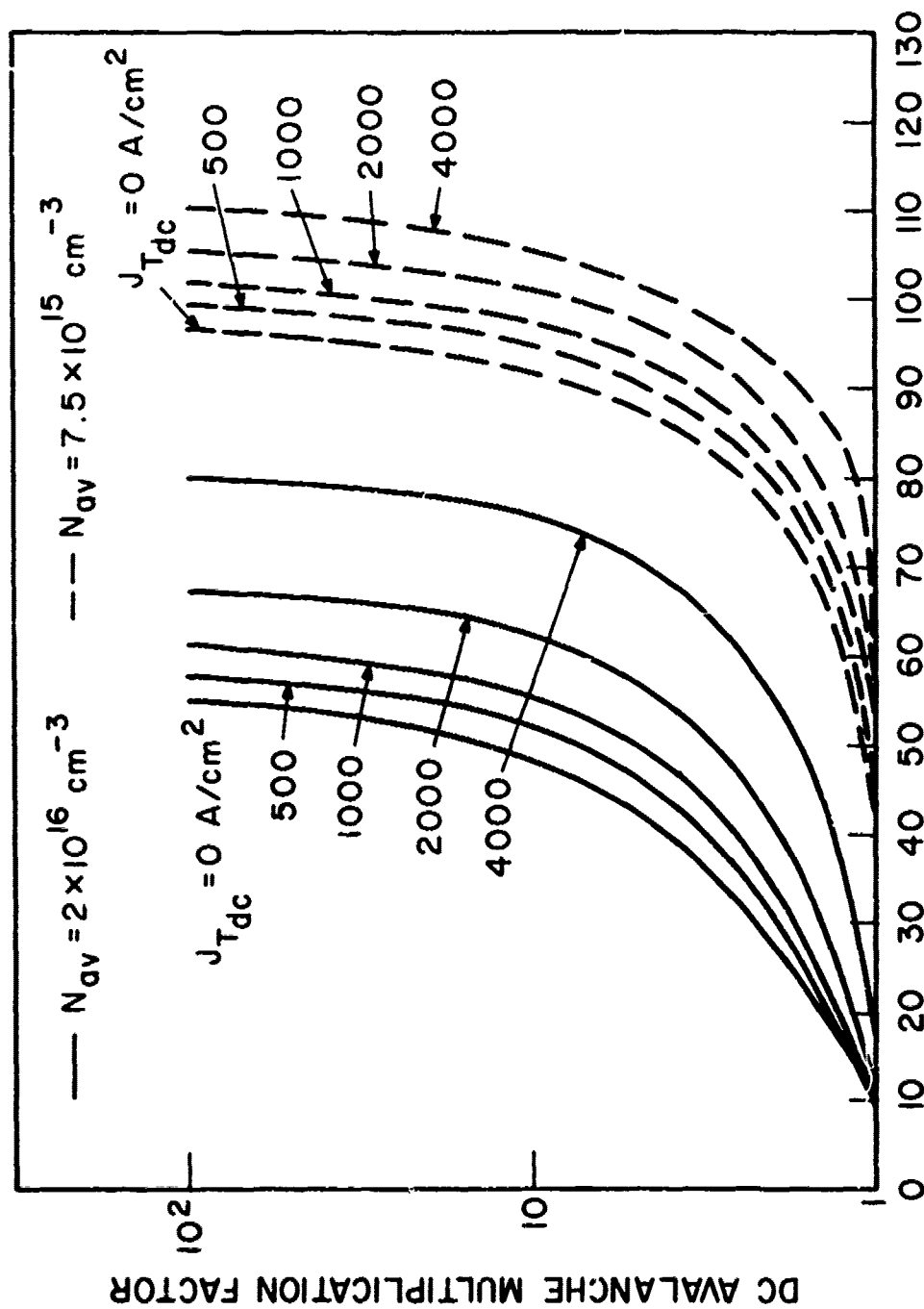
FIG. 2.16 EFFECTS OF SPACE CHARGE. (n-TYPE, Si, $w_{av} = 1 \times 10^{-4}$ cm, $N_{drift} = 2 \times 10^{15}$ cm^{-3}, $w_D = 3 \times 10^{-4}$ cm AND T = 23°C)
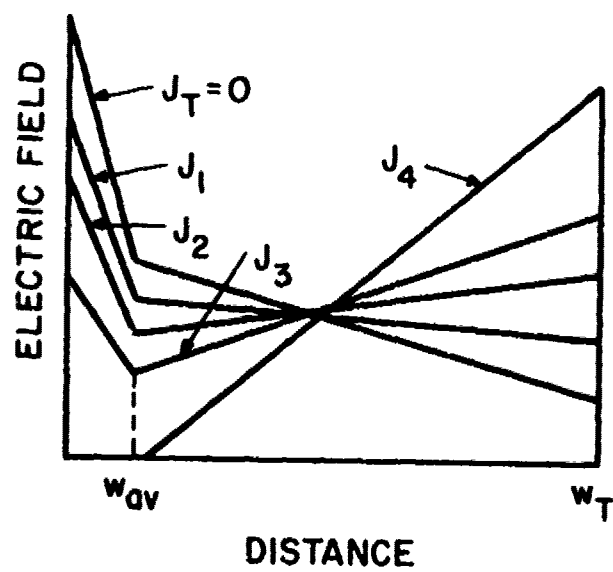
FIG. 2.17 DEPENDENCE OF THE ELECTRIC FIELD PROFILE ON

SPACE-CHARGE DENSITY, N_{av} AND N_{drift}.

$(0 < J_1 < J_2 < J_3)$

M_{A_O} vs. V_T characteristics for making high-gain CATT amplifiers. The effects of collector structural parameters, i.e., N_{av}, N_{drift} and w_D on M_{A_O} vs. V_T characteristics, were investigated and the effects of temperature and space charge were discussed.

CHAPTER III. DEVICE PHYSICS, DC AND SMALL-SIGNAL ANALYTICAL MODELS

3.1 Introduction

This chapter presents a discussion of the physics of CATT
devices, a dc analytic model and a small-signal one. For the dc
device model, the analytical expression for the avalanche multiplication
factor, which was derived in Chapter II, is employed in describing the
current multiplication phenomenon. The effects of high-level
injection in the base region are ignored, but are included in the
large-signal simulation model presented in Chapter IV. The dc space-
charge effects in the collector region are included. The space-charge
effects are different under RF operating conditions and they are
considered in detail in Chapter IV. The electric field in the
collector depletion region is assumed to be sufficient to sustain the
carrier saturation velocity everywhere. The small-signal analytical
model is derived from a first-order Taylor series expansion of dc
quantities and equations about their quiescent values and the lineari-
zation of the resulting equations. This procedure, in general, produces
coupled nonlinear ordinary differential equations in phasor space for
the small-signal variables of interest: particle concentrations,
particle currents, terminal voltages, etc. The small-signal analytical
model does not only include the current multiplication phenomenon, but
also the transit-time effect associated with the base-collector deple-
tion region. The common-base y-parameters are derived and the
unilateral power gain, maximum frequency of oscillation, operating
power gain, transducer power gain, optimum source and load terminations,

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Linvill stability factor, and bandwidth are calculated. A brief discussion of the possibility of operating CATT devices as IMPATT diodes with variable equivalent thermally generated current is given.

3.2 Dc Analytical Model

3.2.1 Carrier Concentration in BJT and CATT Devices. The standard solution for carrier concentrations and currents in the field-free base region of a uniformly doped BJT or CATT structure under low-level injection was first presented by Shockley[2] in the classic paper that introduced the junction transistor in 1949. Shockley's transistor theory still serves as the foundation for all present-day theories of bipolar junction transistor operation including high-level injection, field-aided base transport, the Webster effect and Kirk effects. A one-dimensional uniformly doped npn structure is shown in Fig. 3.1. The minority carrier boundary conditions at the base edge of the emitter-base depletion region and at the base edge of the base-collector depletion region first introduced by Shockley are

$$n(w_2) = n_o \exp (eV_{EB}/kT) \qquad (3.1)$$

and

$$n(w_3) = n_o \exp (- eV_T/kT) \quad , \qquad (3.2)$$

respectively, under normal bias conditions, where V_{EB} is the emitter-base terminal voltage and n_o is the thermal equilibrium concentration. Application of these expressions for the minority carrier boundary conditions to BJT and CATT devices with the emitter-base junction forward biased such that $n(w_2) \gg n_o$, the collector-base junction reverse biased such that $n(w_3) \ll n_o$, and with a base width greater than

-65-
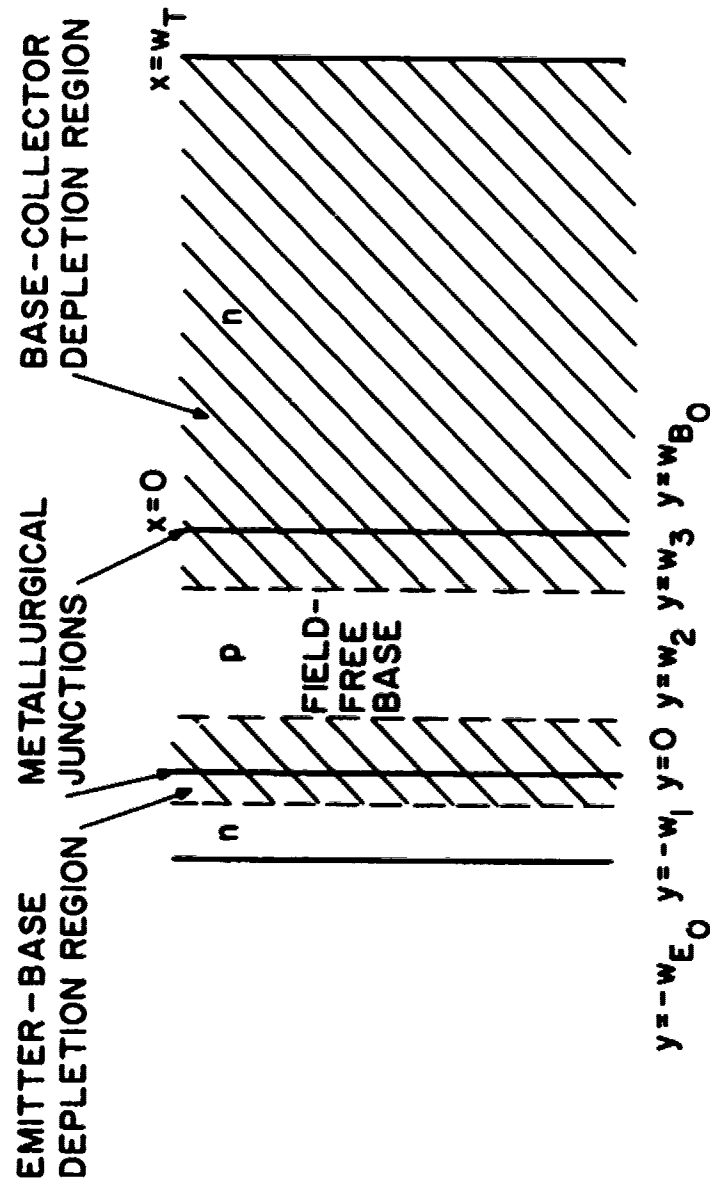
FIG. 3.1 ONE-DIMENSIONAL npn TRANSISTOR STRUCTURE.

several Debye lengths[52] yields a satisfactory description of carrier

transport in the base region under low-level injection. The modifica-

tion required in Eq. 3.1 under high-level injection is discussed in

Chapter IV. If the boundary condition required for the analysis of the

collector region is the minority carrier current density, Eqs. 3.1 and

3.2 are adequate. If the collector boundary condition required is the

minority carrier density, Eq. 3.2 is not appropriate. The requirement

that the minority carrier concentration at the base edge of the base-

collector depletion region be less than the thermal equilibrium

concentration, independent of the minority carrier current density,

is disconcerting at best. An expression for the minority carrier

concentration at the base edge of the base-collector depletion region,

which would result in a smooth transition from diffusion transport to

drift transport that the electrons must undergo in traversing the field-

free base region to the high-field base-collector de tion region, is

given in Chapter IV. For the dc and small-signal analytical models,

the collector boundary condition required is the minority carrier

current density. The case where the base width becomes comparable to

a Debye length has been investigated by McCleer,[52] but it

is of no concern in the modeling of CATT devices.

If a constant base-doping concentration and a low-level emitter

injection are assumed, transport of minority carriers in the field-

free base region can be described by diffusion alone and the dc

electron current density is

$$J_{n_{dc}} = eD_n \frac{dn_{dc}}{dy} ,$$ (3.3)

-67-

where n_{dc} is the dc electron concentration and D_n is the low-field electron diffusion constant. Another relationship which governs the base region electron distribution is the time-independent electron continuity equation

$$0 = \frac{n_{dc} - n_o}{\tau_n} - \frac{1}{e} \frac{dJ_{n_{dc}}}{dy} , \qquad (3.4)$$

where τ_n is the electron lifetime. By substituting Eq. 3.3 into Eq. 3.4, a second-order, constant coefficient, homogeneous ordinary differential equation is obtained whose solution is of the form:

$$n_{dc}(y) - n_o = A e^{-(y-w_2)/L_n} + B e^{(y-w_2)/L_n} ,$$

where $L_n = \sqrt{D_n \tau_n} =$ the electron diffusion length in the base region. The constants A and B can be determined from the boundary conditions given by Eqs. 3.1 and 3.2. Once $n_{dc}(y)$ is found, the electron carrier current is determined from Eq. 3.3. At $y = w_2$ and w_3, the dc electron currents are

$$I_{nE_{dc}} \triangleq I_{n_{dc}}(w_2) = \frac{eD_n A_E}{L_n} \left[[n_{dc}(w_2) - n_o] \coth \left(\frac{w_B}{L_n}\right) \right.$$
$$\left. - [n_{dc}(w_3) - n_o] \operatorname{csch} \left(\frac{w_B}{L_n}\right) \right] \qquad (3.5)$$

and

$$I_{nB_{dc}} \triangleq I_{n_{dc}}(w_3) = \frac{eD_n A_E}{L_n} \left[[n_{dc}(w_2) - n_o] \operatorname{csch}\left(\frac{w_B}{L_n}\right) \right.$$

$$\left. - [n_{dc}(w_3) - n_o] \coth\left(\frac{w_B}{L_n}\right) \right] \quad , \quad (3.6)$$

where A_E is the emitter area, $w_B = w_3 - w_2$,

$$w_2 = \left(\frac{2\varepsilon}{eN_A}\right) \left(\frac{N_D}{N_A + N_D}\right)^{1/2} \frac{1}{\sqrt{V_{BI} - V_{EB_o}}} \quad , \quad (3.7)$$

$$w_3 = w_{B_o} - \left(\frac{2\varepsilon}{eN_A}\right) \left(\frac{N_c}{N_A + N_c}\right)^{1/2} \frac{1}{\sqrt{V_{BI} - V_{T_o}}} \quad , \quad (3.8)$$

w_{B_o} is the metallurgical base width, N_D and N_A are the emitter and base doping levels, V_{EB_o} is the dc emitter-base terminal voltage and V_{BI} is the built-in potential at the proper junction. Under normal bias conditions the following is obtained:

$$I_{nE_{dc}} = \frac{eD_n A_E}{L_n} \left[[n_{dc}(w_2) - n_o] \coth\left(\frac{w_B}{L_n}\right) \right] \quad (3.9)$$

and

$$I_{nB_{dc}} = \frac{eD_n A_E}{L_n} \left[[n_{dc}(w_2) - n_o] \operatorname{csch}\left(\frac{w_B}{L_n}\right) \right] \quad . \quad (3.10)$$

The hole current crossing each junction must be calculated in order to find the total current. Unlike the electron current which links both emitter and collector junctions, the hole currents link only one junction because the base hole current can easily enter or leave

-69-

the base region owing to the ohmic contact to the external terminal. The dc hole current at $y = -w_1$ can be found from Eq. 3.5 by changing all the electron parameters to the corresponding hole parameters in the appropriate regions and by taking the limit of the resulting expression in the limit as $w_B \to \infty$. The result is

$$I_{pE_{dc}} \triangleq I_{p_{dc}}(-w_1) = \frac{eD_p A_E}{L_p} [p_{dc}(-w_1) - p_o] \quad , \qquad (3.11)$$

where D_p = the low-field hole diffusion constant, L_p = the hole diffusion length, p_o = the hole thermal equilibrium concentration, and

$$w_1 = \left(\frac{2\varepsilon}{eN_D}\right) \left(\frac{N_A}{N_D + N_A}\right)^{1/2} \frac{1}{\sqrt{V_{BI} - V_{EB_o}}} \quad . \qquad (3.12)$$

The total dc emitter particle current is given by

$$I_{E_{dc}} = \frac{eD_n A_E}{L_n} \left[[n_{dc}(w_2) - n_o] \coth\left(\frac{w_B}{L_n}\right) \right] + \frac{eD_p A_E}{L_p} [p_{dc}(-w_1) - p_o] \quad .$$
$$(3.13)$$

If $w_B \ll L_n$, Eq. 3.13 can be further reduced to

$$\bar{I}_{E_{dc}} = \frac{eD_n A_E}{w_B} [n_{dc}(w_2) - n_o] + \frac{eD_p A_E}{L_p} [p_{dc}(-w_1) - p_o] \quad . \qquad (3.14)$$

A very important circuit parameter is the short-circuit dc current gain from emitter to collector and it can be written as the product of three parameters as follows:

$$\alpha_o \triangleq \frac{I_{T_{dc}}}{I_{E_{dc}}} = \left(\frac{I_{nE_{dc}}}{I_{E_{dc}}}\right) \left(\frac{I_{nB_{dc}}}{I_{nE_{dc}}}\right) \left(\frac{I_{T_{dc}}}{I_{nB_{dc}}}\right) \quad . \tag{3.15}$$

The first factor is the injection efficiency α_{inj} which gives the fraction of the total emitter current which is made up of the electron carriers. Under normal bias conditions, the dc injection efficiency can be calculated by the following expression:

$$\alpha_{inj_o} = \frac{1}{1 + \left(\frac{D_p}{D_n}\right) \left(\frac{L_n}{L_p}\right) \left(\frac{N_A}{N_D}\right) \tanh \left(\frac{w_B}{L_n}\right)} \quad . \tag{3.16}$$

The second factor is the base transport factor which is given by the following expression:

$$\alpha_{t_o} = \text{sech} \left(\frac{w_B}{L_n}\right) \quad . \tag{3.17}$$

The most accurate two-term expression for α_{t_o} is

$$\alpha_{t_o} = 1 - \frac{1}{2.43} \left(\frac{w_B}{L_n}\right)^2 \quad . \tag{3.18}$$

The third factor is the collector avalanche multiplication factor. For BJTs it is essentially equal to unity. For CATT devices, it is given by Eq. 2.7. For convenience, Eq. 2.7 is stated again as follows:

$$M_{A_o} = \frac{1}{1 - \int_0^{w_T} \alpha_n \left(\exp \int_0^x [\alpha_p(x') - \alpha_n(x')] \, dx'\right) dx} \quad .$$

A good microwave BJT or CATT must, first of all, be a good dc BJT or CATT. From the expressions for α_{inj_o} and α_{t_o}, the design requirements on the emitter and base regions can be deduced.

3.2.2 Base Spreading Resistance.

The cross section of a single-emitter strip in an interdigitated device structure is shown in Fig. 3.2. The base spreading resistance can be calculated by using the following expression:[53]

$$R_B = \left(\frac{w}{12x_{B_1} \sigma_B \ell} + \frac{d}{2x_{B_2} \sigma_B \ell} \right) \frac{1}{\text{number of emitter-base finger pairs}} \quad ,$$

$$(3.19)$$

where the device structural parameters are defined in Fig. 3.2 and the conductivity of the uniformly doped base σ_B is

$$\sigma_B \cong e\mu_p N_A \quad .$$

The variation in R_B due to base region conductivity modulation, which is caused by high concentrations of electron and hole carriers at medium or high-level injection, and base region width modulation, which is caused by the Early effect,[3] has been ignored in the device modeling.

3.2.3 Dc Computer Model.

The dc computer model is snown in Fig. 3.3a. The particle current $I_{E_{dc}}$ flowing in the diode is given by Eq. 3.13. The collector particle current $I_{T_{dc}}$ is calculated by supplying input data $I_{nB_{dc}}$, V_{T_o} and device structural parameters to the computer program DCCP, where $I_{nB_{dc}}$ is given by Eq. 3.10. When avalanche multiplication occurs in the collector depletion region,

FIG 3.2 CROSS SECTION OF SINGLE-EMITTER STRIPE IN AN

INTERDIGITATED TRANSISTOR STRUCTURE.
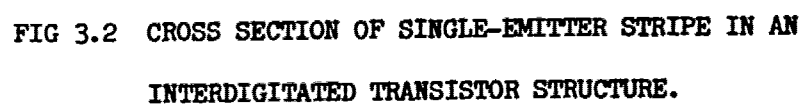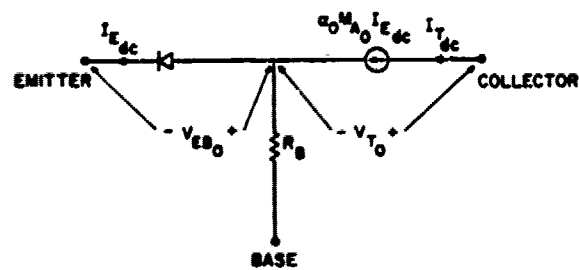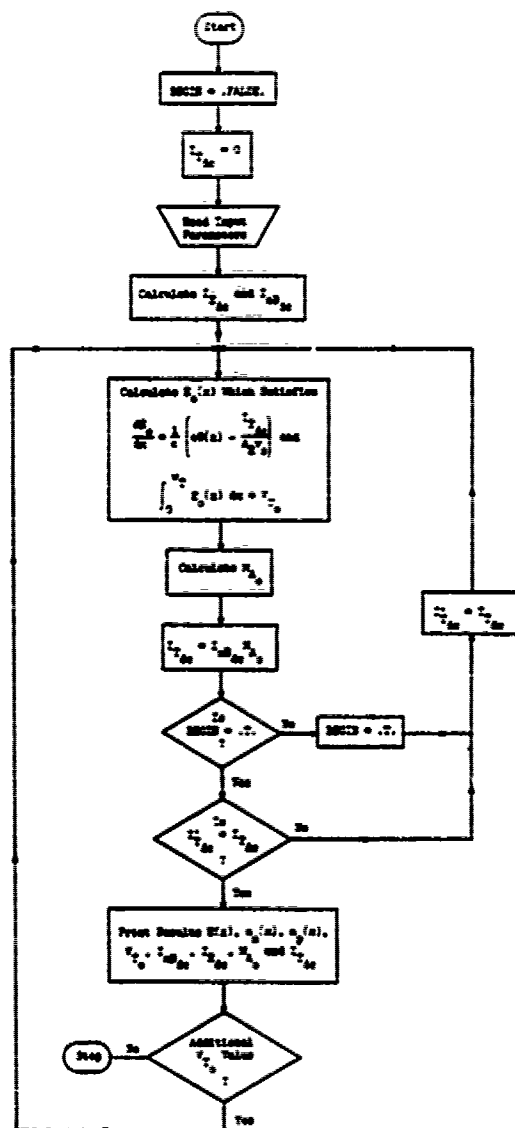
FIG. 3.3 CALCULATION OF COMMON-BASE COLLECTOR CHARACTERISTICS. (a)

DC DEVICE MODEL AND (b) BLOCK DIAGRAM OF DC PROGRAM DCCP.

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electron-hole pairs are created. Electrons, emitter injected and avalanche created, will drift toward the collector contact. Holes, mainly avalanche created, will be transported into the base region and therefore constitute a negative recombination current component.[28,54] They reduce the base current which must be supplied externally. If the avalanche multiplication factor is large enough, the polarity of the base current actually reverses because the avalanche multiplication process in the collector depletion region is providing more holes to the base than are necessary to support recombination in the base and emitter.

The common-base configuration is chosen because the consequences of this avalanche multiplication are straightforward in such an operation. The collector particle current simply equals the product of $I_{nB_{dc}}$ and M_{A_o} . Current $I_{E_{dc}}$ is the parameter of the common-base collector characteristics and it is dependent only on V_{EB_o} , the dc emitter-base terminal voltage. Therefore the common-base characteristics reflect primarily a direct avalanche contribution to the collector current. The consequences of avalanche multiplication are more complicated and subtle when the transistor is operating in the common-emitter configuration since base current $I_{B_{dc}}$ is the parameter of the collector characteristics. The avalanche multiplication factor is dependent on V_{T_o} , $I_{pB_{dc}}$ and $I_{T_{dc}}$ are dependent on $I_{nB_{dc}}$ and M_{A_o} , and $I_{B_{dc}}$ is the difference between the V_{EB_o} -dependent recombination current and $I_{pB_{dc}}$. Therefore, points on an $I_{T_{dc}}$ vs. V_{T_o} (constant $I_{B_{dc}}$) characteristic curve may correspond to different values of $I_{nB_{dc}}$ and such a characteristic curve does not reflect directly the avalanche contribution to the collector current.

Figure 3.3b shows the block diagram of the computer program DCCP which produces the common-base dc collector characteristics. The results of computer program DCCP are given and discussed in Section 3.4.

3.3 Small-Signal Analytical Model

To consider the general ac case, the general one-dimensional time-dependent electron continuity equation must be solved:

$$\frac{\partial n}{\partial t} = \frac{1}{e} \frac{\partial J_n}{\partial y} - \frac{n - n_o}{\tau_n} \ . \tag{3.20}$$

The following is obtained using Eqs. 3.3 and 3.20

$$\frac{\partial^2 n}{\partial y^2} - \frac{1}{L_n^2} (n - n_o) = \frac{1}{D_n} \frac{\partial n}{\partial t} \ , \tag{3.21}$$

and the solution of Eq. 3.21 is of the following form:

$$n(y,t) = n_{dc}(y) + n_1(y)e^{j\omega t} \tag{3.22}$$

when the sources are sinusoidal with frequency ω. The first term on the right-hand side corresponds to the dc solution. The second term is the ac variation and is in the form of a product of two terms. This is a frequently used method of solving partial differential equations. It is assumed in Eq. 3.22 that the minority carrier concentration varies sinusoidally with the same frequency as that of the driving sources. When Eq. 3.22 is substituted into Eq. 3.21, the following two equations are obtained:

$$\frac{d^2 n_{dc}}{dy^2} - \frac{n_{dc} - n_o}{L_n^2} = 0 \tag{3.23}$$

and

$$\frac{d^2 n_1}{dy^2} - \left(\frac{1 + j\omega\tau_n}{L_n^2}\right) n_1 = 0 \quad . \qquad (3.24)$$

The boundary condition in Eq. 3.1 is quite general and is not restricted to dc applied voltages. Thus if the emitter-base junction voltage is composed of a dc voltage V_{EB_0} and an ac voltage $V_{EB_1} e^{j\omega t}$, the minority carrier concentration on the base side of the emitter-base junction is

$$n(w_2, t) = n_0 e^{eV_{EB_0}/kT} + n_0 e^{eV_{EB_0}/kT} \frac{eV_{EB_1} e^{j\omega t}}{kT} \quad , \qquad (3.25)$$

where the first term on the right-hand side is the dc value and the second term is the ac value. Equation 3.25 is valid provided that

$$|V_{EB_1}| \ll \frac{kT}{e} \quad , \qquad (3.26)$$

which represents the small-signal assumption.

Note that the form of the differential equation for the ac electron density in Eq. 3.24 is the same as that for the dc electron density. This suggests that the ac solution can be obtained from the dc solution directly by the use of some simple transformations. The ac electron particle currents at $y = w_2$ and w_3 are found to be

$$I_{nE_1} e^{j\omega t} = \frac{e^2 D_n A_E}{kT} \frac{\sqrt{1 + j\omega\tau_n}}{L_n} \times V_{EB_1} e^{j\omega t} n_{dc}(w_2) \coth\left(\frac{\sqrt{1 + j\omega\tau_n}}{L_n} w_B\right)$$

$$(3.27)$$

and

$$I_{nB_1} e^{j\omega t} = \frac{e^2 D_n A_E}{kT} \frac{\sqrt{1 + j\omega\tau_n}}{L_n} \times V_{EB_1} e^{j\omega t} n_{dc}(w_2) \operatorname{csch}\left[\frac{\sqrt{1 + j\omega\tau_n}}{L_n} w_B\right]$$

$$(3.28)$$

under normal bias conditions. The depletion region boundaries w_2 and w_3 are determined by Eqs. 3.7 and 3.8 with V_{EB} and V_T set at their respective dc values. The hole current at $y = -w_1$ is given by

$$I_{pE_1} e^{j\omega t} = \frac{e^2 D_p A_E}{kT} \frac{\sqrt{1 + j\omega\tau_p}}{L_p} V_{EB_1} e^{j\omega t} p_{dc}(-w_1) \quad . \quad (3.29)$$

Physically, $I_{nB_1} e^{j\omega t}$ is the time-dependent electron current injected into the base-collector depletion region. The expressions which approximate the physics in the collector region under small-signal conditions are derived next. Finally, the small-signal y-parameters of the common-base configuration are derived.

Most of the carrier generation due to avalanche multiplication occurs in a narrow high-field portion of the collector region, which is named the generation region, whose width is w_{av}. The remainder of the collector region is the drift region whose width is w_D. The basic device equations in the generation region are

$$\frac{\partial E}{\partial x} = -\frac{e}{\epsilon}(N_D^+ - N_A^- + p - n) \quad , \quad (3.30)$$

$$J_n = e v_s n \quad , \quad (3.31)$$

$$J_p = e v_s p \quad , \quad (3.32)$$

$$\frac{\partial n}{\partial t} = -\frac{1}{e} \frac{\partial J_n}{\partial x} + \alpha v_s (n + p) \quad (3.33)$$

and

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$$\frac{\partial p}{\partial t} = \frac{1}{e} \frac{\partial J_p}{\partial x} + \alpha v_s (n + p) \ , \qquad (3.34)$$

where $\alpha_n = \alpha_p = \alpha$ and $v_{ns} = v_{ps} = v_s$ are assumed. The convention for the direction of particle flow and electric field for n-type CATT devices is shown in Fig. 3.4. The addition of Eqs. 3.33 and 3.34, substitution of Eqs. 3.31 and 3.32 and integration from $x = 0$ to $x = w_{av}$ yields

$$\frac{w_{av}}{v_s} \frac{dJ_g}{dt} = (J_p - J_n) \Big|_0^{w_{av}} + 2J_g \int_0^{w_{av}} \alpha \, dx \ ,$$

where J_g is the total conduction current in the generation region. With boundary conditions

$$J_n(0,t) = J_{nB}(t) + J_{c_{ns}} \qquad (3.35)$$

and

$$J_p(w_{av},t) = J_{c_{ps}} \ , \qquad (3.36)$$

the preceding equation becomes

$$\frac{dJ_g(t)}{dt} = \frac{2J_g}{\tau_g} \left(\int_0^{w_{av}} \alpha \, dx - 1 \right) + \frac{2\left(J_{nB}(t) + J_{c_{ns}} + J_{c_{ps}} \right)}{\tau_g} \ ,$$

$$(3.37)$$

where $\tau_g \overset{\Delta}{=} w_{av}/v_s$. With the small-signal assumptions

$$\alpha = \alpha_0 + \alpha' E_{g_1} e^{j\omega t} \ ,$$

$$J_g = J_{g_{dc}} + J_{g_1} e^{j\omega t} \ ,$$
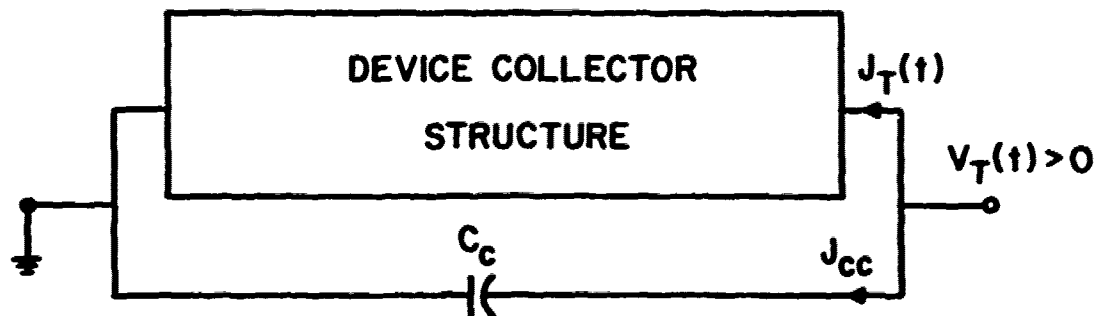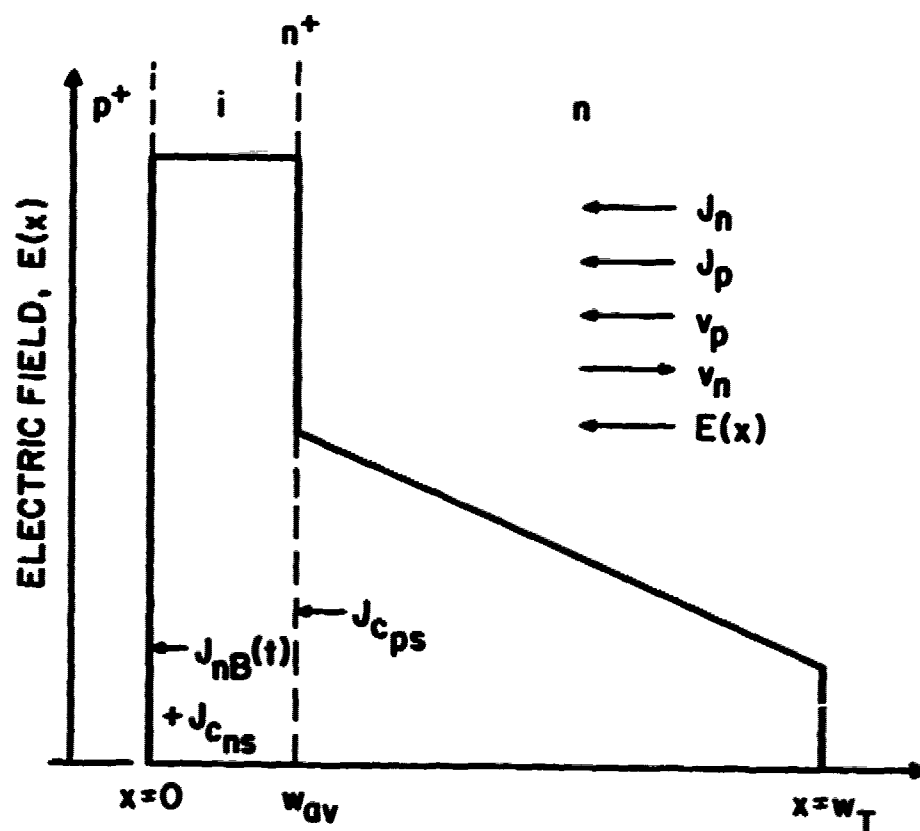
FIG. 2.4 (a) GENERAL DEVICE COLLECTOR STRUCTURE AND

(b) ELECTRIC FIELD AND CURRENT CONVENTIONS.

$$E_{\mathcal{E}} = E_{\mathcal{E}_0} + E_{\mathcal{E}_1} e^{j\omega t}$$

and

$$J_{nB} = J_{nB_{dc}} + J_{nB_1} e^{j\omega t} \quad ,$$

the following can be obtained from Eq. 3.37

$$J_{\mathcal{E}_{dc}} = \frac{J_{nB_{dc}} + J_{c_{ns}} + J_{c_{ps}}}{1 - \int_0^{w_{av}} \alpha_0 \, dx} \quad , \qquad (3.38)$$

the dc equation, and

$$J_{\mathcal{E}_1} = \frac{J_{\mathcal{E}_{dc}} \int_0^{w_{av}} \alpha' E_{\mathcal{E}_1} \, dx + J_{nB_1}}{1 - \int_0^{w_{av}} \alpha_0 \, dx + j \frac{\omega \tau_{\mathcal{E}}}{2}} \quad , \qquad (3.39)$$

the ac equation, where the second-and higher-order terms are neglected. If the collector has a Read-type structure and negligible space-charge effect, both $E_{\mathcal{E}_0}$ and $E_{\mathcal{E}_1}$ are constants. Equation 3.34 becomes

$$J_{\mathcal{E}_1} = \frac{J_{\mathcal{E}_{dc}} \left(\frac{b}{E_{\mathcal{E}_0}^2}\right) \left(1 - \frac{1}{M_{A_0}}\right) E_{\mathcal{E}_1} + J_{nB_1}}{\frac{1}{M_{A_0}} + j \frac{\omega \tau_{\mathcal{E}}}{2}} \quad , \qquad (3.40)$$

where $M_{A_0} = 1/(1 - \alpha_0 w_{av})$. By using the analytical expression for the ionization rate

$$\alpha_0 = A e^{-b/E_{\mathcal{E}_0}} \quad ,$$

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Eq. 3.40 can be written as

$$J_{g_1} =$$

$$\frac{(J_{nB_{dc}} + J_{c_{ns}} + J_{c_{ps}})\left(M_{A_o} - 1\right)\dfrac{\left[\ln(w_{av}A) - \ln\left(1 - \dfrac{1}{M_{A_o}}\right)\right]^2}{b} E_{g_1} + J_{nB_1}}{\left(\dfrac{1}{M_{A_o}} + j\,\dfrac{\omega\tau_g}{2}\right)} \;.$$

$$(3.41)$$

Equation 3.41 gives the current density at the interface between the generation region and the drift region.

If a saturated drift velocity v_s and zero carrier generation in the drift region are assumed, the ac conduction current density $J_{D_1}(x)\, e^{j\omega t}$ in the drift region propagates as an unattenuated wave at this drift velocity

$$J_{D_1}(x) = J_{g_1}\, e^{-j\omega(x-w_{av})/v_s} \;, \qquad (3.42)$$

where the exponential term represents the phase delay. The induced ac collector terminal current density is

$$J_{T_1} = \frac{1}{v_D}\int_{w_{av}}^{w_T} J_{D_1}(x)\, dx$$

$$= J_{g_1}\,\frac{\sin\dfrac{\theta_D}{2}}{\dfrac{\theta_D}{2}}\, e^{-j(\theta_D/2)} \;, \qquad (3.43)$$

where $\theta_D \triangleq \omega w_D/v_s$ and $J_T(t) = J_{T_{dc}} + J_{T_1}\, e^{j\omega t}$.

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The voltage across the base-collector terminal is $V_T = V_{T_0} + V_{T_1} e^{j\omega t}$, where V_{T_1} is the ac voltage component. The ac electric field is constant throughout the collector region if the space-charge effects of J_{g_1} and J_{D_1} are ignored (see Fig. 3.5). The ac electric field in the generation region is

$$E_{g_1} = \frac{V_{T_1}}{w_T} .$$ (3.44)

By combining Eqs. 3.41, 3.43 and 3.44, the following expression for I_{T_1} can be derived:

$$I_{T_1} = \left\{ \frac{(J_{nB_{dc}} + J_{c_{ns}} + J_{c_{ps}})\left(M_{A_0} - 1\right)\dfrac{\left[\ln(w_{av}A) - \ln\left[1 - \dfrac{1}{M_{A_0}}\right]\right]^2}{bw_T}}{\dfrac{1}{M_{A_0}} + j\,\dfrac{\omega\tau_g}{2}} V_{T_1} \right.$$

$$\left. + \frac{1}{\dfrac{1}{M_{A_0}} + j\,\dfrac{\omega\tau_g}{2}} J_{nB_1} \right\} \frac{A_E \sin\dfrac{\theta_D}{2}}{\dfrac{\theta_D}{2}} e^{-j(\theta_D/2)} .$$ (3.45)

The preceding expression is a more complete description of the small-signal device physics than the formulation of Winstanley and Carroll[35] and it is very similar to the expression derived by Quang[37] except that M_{A_0} is assumed to be infinity in the latter case. The total ac collector terminal current is given by

$$I_{c_1} = I_{T_1} + j\omega C_c V_{T_1} ,$$ (3.46)

where $C_c = \epsilon A_E/w_T$. The small-signal device model is given in Fig. 3.6a and the small-signal circuit model is given in Fig. 3.6b. The circuit

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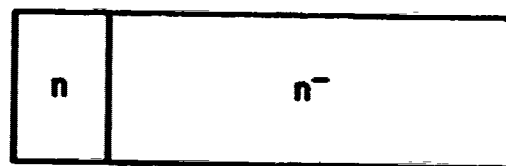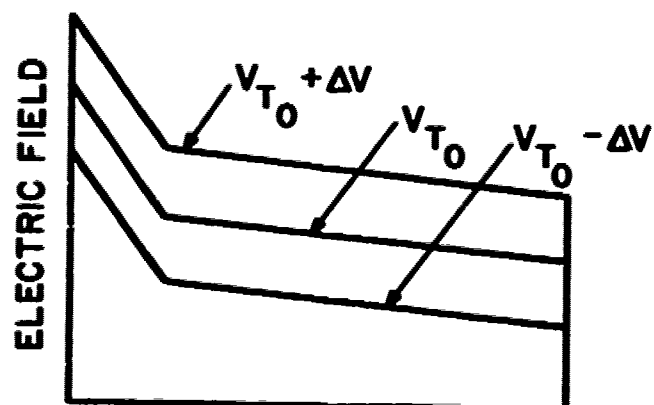
FIG. 3.5 ELECTRIC FIELD PROFILE UNDER RF CONDITIONS.
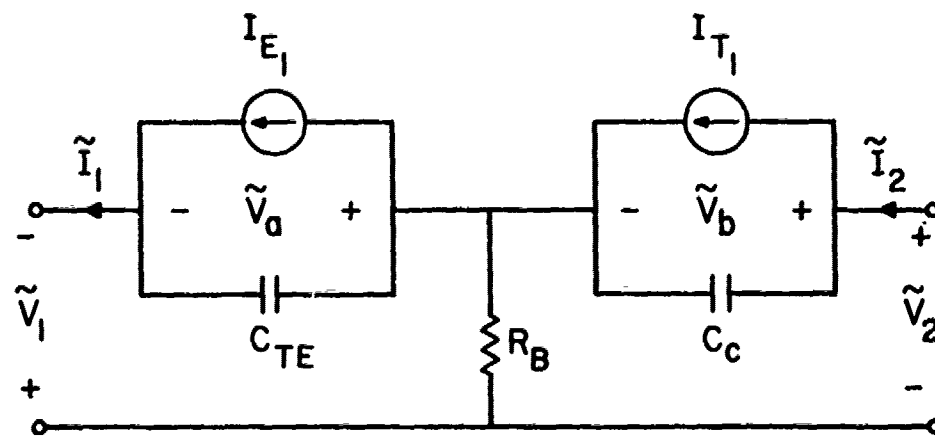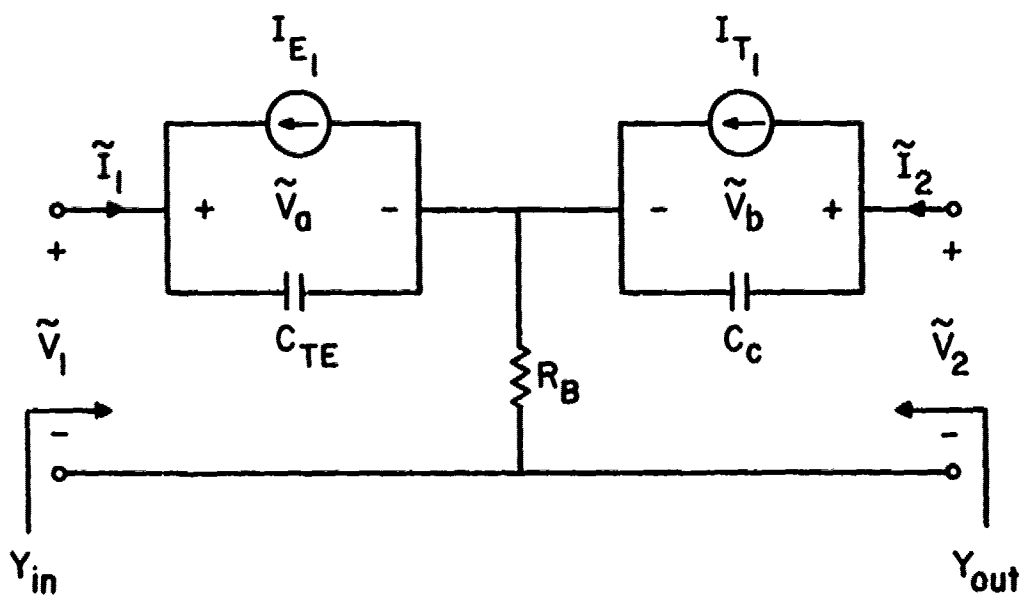
FIG. 3.6 SMALL-SIGNAL MODELS. (a) DEVICE MODEL
AND (b) CIRCUIT MODEL.

element C_{TE} is the emitter-base transition region capacitance and its value is

$$C_{TE} = \frac{\varepsilon A_E}{w_1 + w_2}\Bigg|_{V_{EB_o}} \quad , \tag{3.47}$$

where w_1 and w_2 are calculated by using Eqs. 3.7 and 3.12. If $\tilde{I}_1$ and $\tilde{I}_2$, the total ac emitter current and the total ac collector current, are written as

$$\tilde{I}_1 = y_{11}\tilde{V}_a + y_{12}\tilde{V}_b \tag{3.48}$$

and

$$\tilde{I}_2 = y_{21}\tilde{V}_a + y_{22}\tilde{V}_b \quad , \tag{3.49}$$

where $\tilde{I}_{1,2}$ and $\tilde{V}_{1,2}$ are ac voltages across the terminals, then using Eqs. 3.27 through 3.29 and Eqs. 3.45 and 3.46 yields the following expressions:

$$y_{11} = \frac{e}{kT}\left[\frac{I_{nE_{dc}}\sqrt{1 + j\omega\tau_n}\tanh{(w_B/L_n)}}{\tanh\left(\frac{w_B\sqrt{1 + j\omega\tau_n}}{L_n}\right)} + I_{pE_{dc}}\sqrt{1 + j\omega\tau_p}\right] + j\omega C_{TE} \quad , \tag{3.50}$$

$$y_{12} = 0 \quad , \tag{3.51}$$

$$y_{21} = -\frac{e}{kT}\frac{I_{nE_{dc}}\sqrt{1 + j\omega\tau_n}\tanh\left(\frac{w_B}{L_n}\right)}{\sinh\left(\frac{w_B\sqrt{+ j\omega\tau_n}}{L_n}\right)}\frac{1}{\frac{1}{M_{A_o}} + j\frac{\omega\tau_g}{2}}\frac{\sin\frac{\theta_D}{2}}{\frac{\theta_D}{2}}e^{-j(\theta_D/2)} \tag{3.52}$$

and

$$y_{22} = \frac{(I_{nB_{dc}} + I_{c_{ns}} + I_{c_{ps}})(M_{A_O} - 1)\left[\ln(w_{av}A) - \ln\left(1 - \frac{1}{M_{A_O}}\right)\right]^2}{\left(\frac{1}{M_{A_O}} + j\,\frac{\omega\tau}{2}\,g\right)(w_T b)}$$

$$\cdot\ \frac{\sin\frac{\theta_D}{2}}{\frac{\theta_D}{2}}\,e^{-j(\theta_D/2)} + j\omega C_c \quad . \quad (3.53)$$

If $\tilde{y}$-parameters are defined as

$$\tilde{I}_1 = \tilde{y}_{11}\tilde{V}_1 + \tilde{y}_{12}\tilde{V}_2 \tag{3.54}$$

and

$$\tilde{I}_2 = \tilde{y}_{21}\tilde{V}_1 + \tilde{y}_{22}\tilde{V}_2 \quad , \tag{3.55}$$

it can be shown that

$$\tilde{y}_{11} = \frac{y_{11}(1 + R_B y_{22})}{1 + R_B(y_{11} + y_{21} + y_{22})} \quad , \tag{3.56}$$

$$\tilde{y}_{12} = -\frac{R_B y_{11} y_{22}}{1 + R_B(y_{11} + y_{21} + y_{22})} \quad , \tag{3.57}$$

$$\tilde{y}_{21} = \frac{y_{21} - R_B y_{11} y_{22}}{1 + R_B(y_{11} + y_{21} + y_{22})} \tag{3.58}$$

and

$$\tilde{y}_{22} = \frac{(1 + R_B y_{11})y_{22}}{1 + R_B(y_{11} + y_{21} + y_{22})} \quad . \tag{3.59}$$

The input and output admittances, expressed in terms of $\tilde{y}_{ij}$, are

$$Y_{in} \;=\; G_{in} + jB_{in} \;=\; \tilde{y}_{11} - \frac{\tilde{y}_{12}\tilde{y}_{21}}{\tilde{y}_{22} + Y_L} \tag{3.60}$$

and

$$Y_{out} \;=\; G_{out} + jB_{out} \;=\; \tilde{y}_{22} - \frac{\tilde{y}_{12}\tilde{y}_{21}}{\tilde{y}_{11} + Y_S} \;, \tag{3.61}$$

where Y_L and Y_S are the load and the source admittances, respectively. By using the derived $\tilde{y}$-parameters, many small-signal device performance capabilities can be calculated.

The passivity condition[55] is given as follows:

$$\tilde{g}_{11} \gtreqqless 0 \;, \tag{3.62}$$

$$\tilde{g}_{22} \gtreqqless 0 \;, \tag{3.63}$$

$$\tilde{g}_{11}\tilde{g}_{22} - \tilde{g}_{12}\tilde{g}_{21} - \frac{|\tilde{y}_{21} - \tilde{y}_{12}|^2}{4} \gtreqqless 0 \tag{3.64}$$

and

$$\tilde{g}_{11}\tilde{g}_{22} + \tilde{b}_{12}\tilde{b}_{21} - \frac{|\tilde{y}_{21} + \tilde{y}_{12}|^2}{4} \gtreqqless 0 \;, \tag{3.65}$$

where $\tilde{g}_{ij}$ and $\tilde{b}_{ij}$ are the real and imaginary parts of $\tilde{y}_{ij}$. If any of these conditions are violated, the device is active instead of passive. The passivity condition in Eq. 3.64 can be written as

$$1 - U \gtreqqless 0 \;,$$

where

$$U = \frac{|\tilde{y}_{21} - \tilde{y}_{12}|^2}{4(\tilde{g}_{11}\tilde{g}_{22} - \tilde{g}_{12}\tilde{g}_{21})} \quad . \tag{3.66}$$

Thus, if $g_{11} \overset{\geq}{=} 0$ and $g_{22} \overset{\geq}{=} 0$ and $0 \overset{\leq}{=} U \overset{\leq}{=} 1$, the device is passive. If $U > 1$, the device is active. The quantity U is a measure of the degree of activity. The maximum frequency of oscillation ω_{max} is defined as

$$U(\omega_{max}) = 1 \quad . \tag{3.67}$$

The Linvill stability factor S is[55]

$$S = \frac{|\tilde{y}_{12}\tilde{y}_{21}|}{2\tilde{g}_{11}\tilde{g}_{22} - \tilde{g}_{12}\tilde{g}_{21} + \tilde{b}_{12}\tilde{b}_{21}} \quad . \tag{3.68}$$

When $1 < S < \infty$ or when $S < 0$, the device is potentially unstable, that is, oscillation can occur for certain selected passive terminations. When $0 < S < 1$, the device is inherently stable, that is, no passive terminations can cause oscillation without suitable external feedback. When $S = 1$, the device is critically stable (see Fig. 3.7 for the definitions of various powers). The operating power gain is

$$G_p = \frac{P_{out}}{P_{in}} = \frac{|\tilde{y}_{21}|^2 G_L}{|\tilde{y}_{22} + Y_L|^2 \, \mathrm{Re}\left(\tilde{y}_{11} - \frac{\tilde{y}_{12}\tilde{y}_{21}}{\tilde{y}_{22} + Y_L}\right)} \quad , \tag{3.69}$$

where Re is the real part of any complex number and $G_L = \mathrm{Re}(Y_L)$. If the amplifier is inherently stable, the maximum operating gain is achieved when the load is

$$G_{L_{opt}} = \frac{1}{2\tilde{g}_{11}} \sqrt{[2\tilde{g}_{11}\tilde{g}_{22} - \mathrm{Re}(\tilde{y}_{12}\tilde{y}_{21})]^2 - |\tilde{y}_{12}\tilde{y}_{21}|^2} \tag{3.70}$$
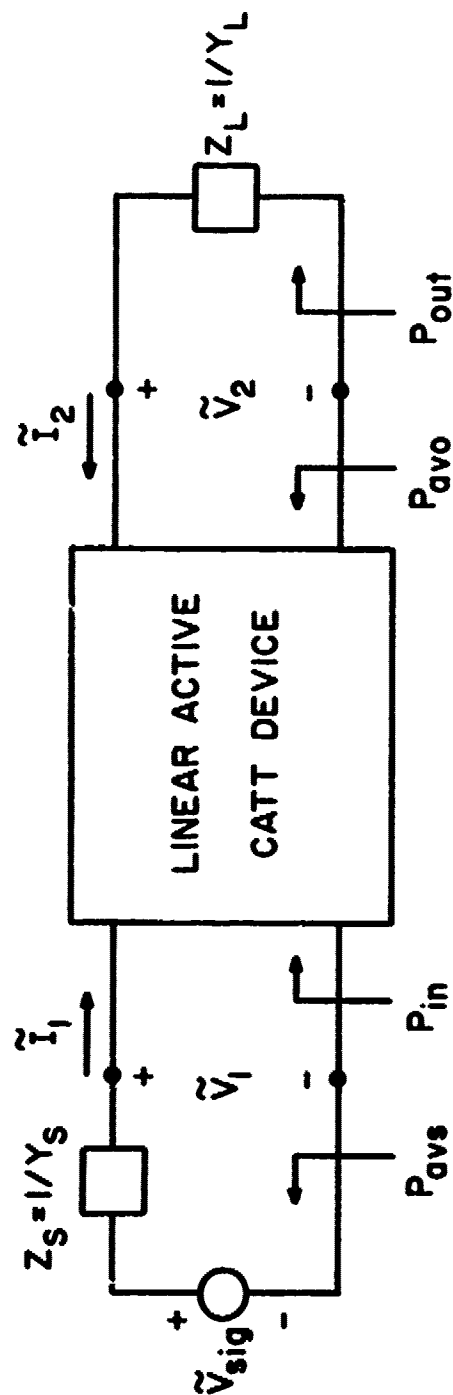
FIG 3.7 LINEAR ACTIVE CATT CIRCUIT. (P_{avs} = THE POWER AVAILABLE FROM THE SOURCE

AND P_{avo} = THE POWER AVAILABLE TO THE LOAD)

and

$$B_{L_{opt}} = \frac{Im(\tilde{y}_{12}\tilde{y}_{21})}{2\tilde{g}_{11}} - \tilde{b}_{22} \quad , \tag{3.71}$$

where Im is the imaginary part of any complex number. Substitution of
Eqs. 3.70 and 3.71 into Eq. 3.60 yields the input admittance Y_{in} with
$Y_L = Y_{L_{opt}}$. In order to deliver maximum power to the device the input
admittance must be the conjugate of the source admittance; therefore,
when Y_S is given by

$$G_{S_{opt}} = Re(Y_S) = \frac{1}{2\tilde{g}_{22}} \sqrt{[2\tilde{g}_{11}\tilde{g}_{22} - Re(\tilde{y}_{12}\tilde{y}_{21})]^2 - |\tilde{y}_{12}\tilde{y}_{21}|^2}$$

$$\tag{3.72}$$

and

$$B_{S_{opt}} = \frac{Im(\tilde{y}_{12}\tilde{y}_{21})}{2\tilde{g}_{22}} - \tilde{b}_{11} \quad , \tag{3.73}$$

maximum power as well as maximum operating power gain are achieved.

The optimum terminations for a CATT amplifier are usually obtained
by adjusting the values of the components in the matching networks.
Ease of tunability, or alignability, depends on fractional change in
input admittance compared to the fractional change in load admittance
and on the fractional change in output admittance compared to the
fractional change in source admittance. When the fractional changes in
input and output admittances are small, it is not necessary to alternate
many times between input and output tuning to achieve the desired
condition of operation. In terms of the $\tilde{y}$-parameters, the input

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tunability is given by

$$\delta = \left| \frac{dY_{in}/Y_{in}}{dY_L/Y_L} \right| = \frac{|\tilde{y}_{12}\tilde{y}_{21}||Y_L|}{|\tilde{y}_{22} + Y_L||\tilde{y}_{11}(\tilde{y}_{22} + Y_L) - \tilde{y}_{12}\tilde{y}_{21}|} \quad . \quad (3.74)$$

Tuning is easier as δ is made smaller. In order to achieve good tunability, the load admittance may be chosen such that $Y_L \gg \tilde{y}_{22}$ in order to make $\delta < 0.3$. Then Eq. 3.74 becomes

$$\delta = \frac{|\tilde{y}_{12}\tilde{y}_{21}|}{|\tilde{y}_{11}||Y_L|} \quad . \quad (3.75)$$

The output power varies with frequency partly because the device parameters are frequency dependent but primarily because the conditions for a conjugate match at the input and output ports may not be obtained except at the design-center frequency f_o. The amplifier bandwidth can be approximated under certain conditions from the inherent bandwidth BW^i at either port given by[55]

$$BW_{in}^i = \frac{2f_o G_{S_{opt}}}{|B_{S_{opt}}|} \quad (3.76)$$

for the input circuit, and by

$$BW_{out}^i = \frac{2f_o G_{L_{opt}}}{|B_{L_{opt}}|} \quad (3.77)$$

for the output circuit. Inherent bandwidth is the name given to the bandwidth that is obtained in the conjugate matching situation where the optimum terminations are determined only by the device parameters. It often happens that $BW_{in}^i \gg BW_{out}^i$ and in such cases the overall

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amplifier bandwidth is determined by the output circuit. Bandwidths

are inversely proportional to B_L and B_S. Therefore, the input or output

bandwidth can be decreased below the inherent bandwidth by adding shunt

capacitances C_L or C_S across the input and output terminals without

affecting the optimum termination conductances. Maximum operating

power gain is still achieved. When an inherent bandwidth is too small

for a particular application, the bandwidth can be increased by raising

the termination conductances. This means that additional shunt resistance

can be connected across the input or output terminals. The power gain

is decreased when the bandwidth is increased.

When the transistor parameters are such that potential instability

occurs, a certain output load causes the input conductance to be zero

or negative and the power gain to be infinite. A mismatching technique

can be used to ensure the stability of the amplifier circuitry.

3.4 Dc and Small-Signal Results

Typical common-base characteristics of CATT devices are shown in

Figs. 3.8 through 3.10. Carrier multiplication is evident from the

common-base characteristics. Figures 3.8 through 3.10 represent three

CATT devices with different doping densities in the avalanche multipli-

cation region. The effects of N_{av} are observed in the different rates

of increase in $J_{T_{dc}}$ as a function of V_{T_o}, different breakdown voltages

and different punch-through voltages. The effects of w_{av}, N_{drift} and

w_D on the common-base characteristics can also be investigated by

applying the computer program DCCP.

It can be inferred from Figs. 3.8 through 3.10 that common-base

biased CATT devices can be employed to product current amplification,

and the device in Fig. 3.8 is suitable for such applications. The dc
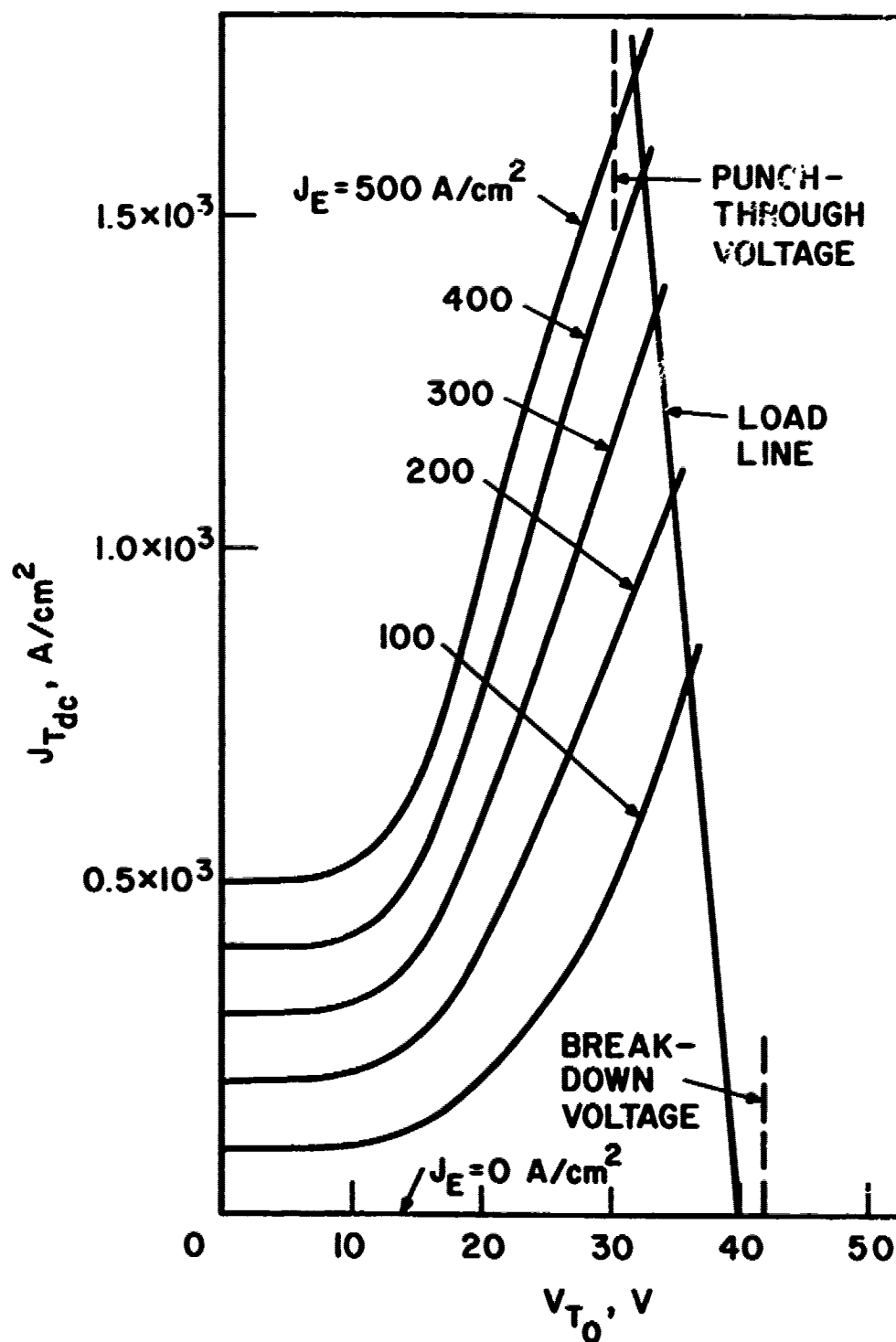
FIG. 3.8 COMMON-BASE CHARACTERISTICS. (n-TYPE, Si, w_{av} = 1×10^{-4} cm, N_{av} = 2.5×10^{16} cm^{-3}, w_D = 3×10^{-4} cm, N_{drift} = 2×10^{15} cm^{-3} AND T = 300°K)

FIG. 3.9 COMMON-BASE CHARACTERISTICS. (n-TYPE, Si,

$v_{av} = 1 \times 10^{-4}$ cm, $N_{av} = 1.5 \times 10^{16}$ cm^{-3},

$v_D = 3 \times 10^{-4}$ cm, $N_{drift} = 2 \times 10^{15}$ cm^{-3}
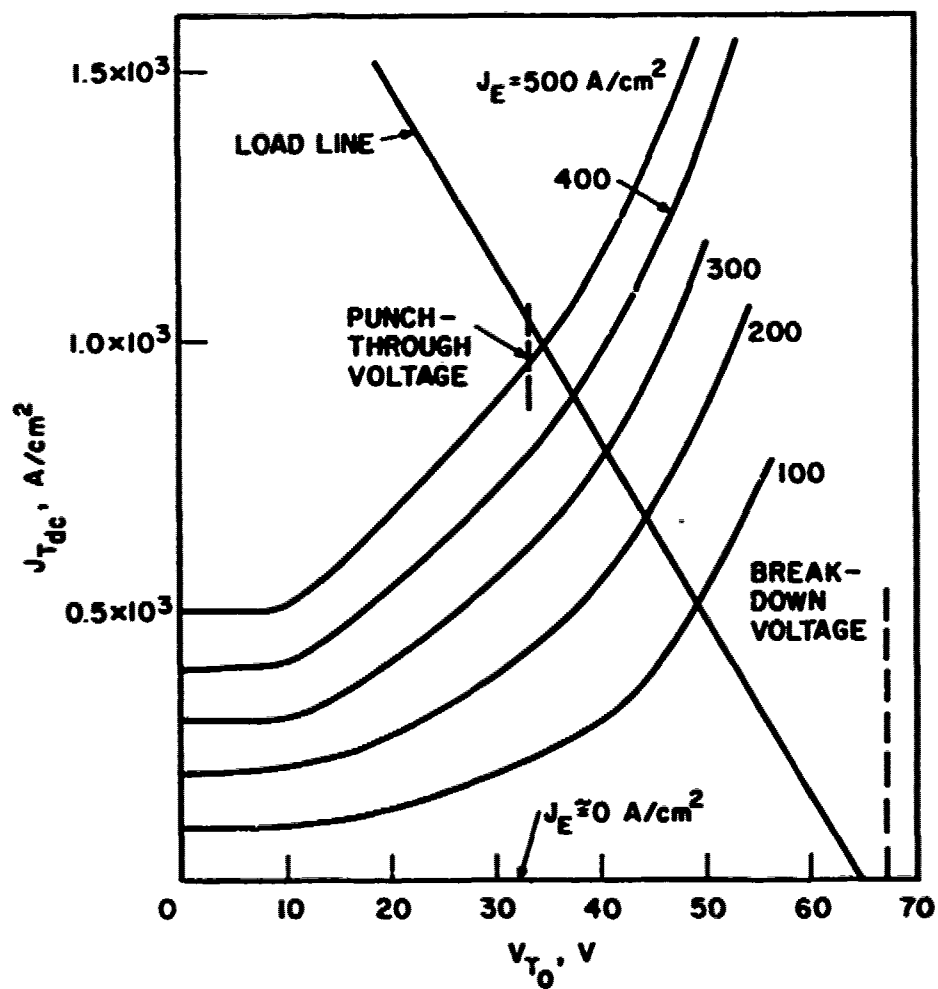
AND T = 300°K)

FIG. 3.10 COMMON-BASE CHARACTERISTICS. (n-TYPE, Si,

$w_{av} = 1 \times 10^{-4}$ cm, $N_{av} = 2 \times 10^{16}$ cm^{-3},

$w_D = 3 \times 10^{-4}$ cm, $N_{drift} = 2 \times 10^{15}$ cm^{-3}

AND T = 300°K)

base-collector bias should be set close to the breakdown voltage as long as the thermal limitation is not exceeded and the load resistor is small (see Fig. 3.8). For applications in voltage amplifications, the device in Fig. 3.9 is more suitable. In fact, a device with a lightly doped, uniform collector structure has even greater capability for voltage amplification. The dc base-collector bias should be set close to the breakdown voltage in Class C operation and set close to $(1/2)(V_B + V_{PT})$ in Class A operation. The upper and lower limits of V_T are V_B and V_{PT}, respectively. It is assumed that a punched-through or nearly punched-through collector is a required operating condition. The load resistor is large. For applications in power amplification, the device in Fig. 3.10 is more suitable where both a large current multiplication and large V_{RF} can result with proper dc bias and load resistor applied.

A computer program SSCP was written which is capable of determining the small-signal common-base y-parameters of CATT amplifiers. Typical U vs. frequency and maximum operating power gain vs. frequency plots are shown in Figs. 3.11 through 3.14. The quantity U is plotted over the frequency range in which $U \gtreqqless 0$. Note that the device can still be active even if $U < 0$ as long as either $g_{11} < 0$ or $g_{22} < 0$. Maximum operating power gain is displayed over the entire frequency range in which the device is capable of power amplification.

From Figs. 3.11 through 3.14 it is observed that the maximum operating power gain at $M_{A_o} > 1$ is much lower than the maximum operating power gain at $M_{A_o} = 1$, but the gain at $M_{A_o} > 1$ is constant over a very wide range of frequencies. If $V_{EB_o} \lesssim 0.8$ V, avalanche multiplication will increase f_{max}, the maximum frequency at which an operating power
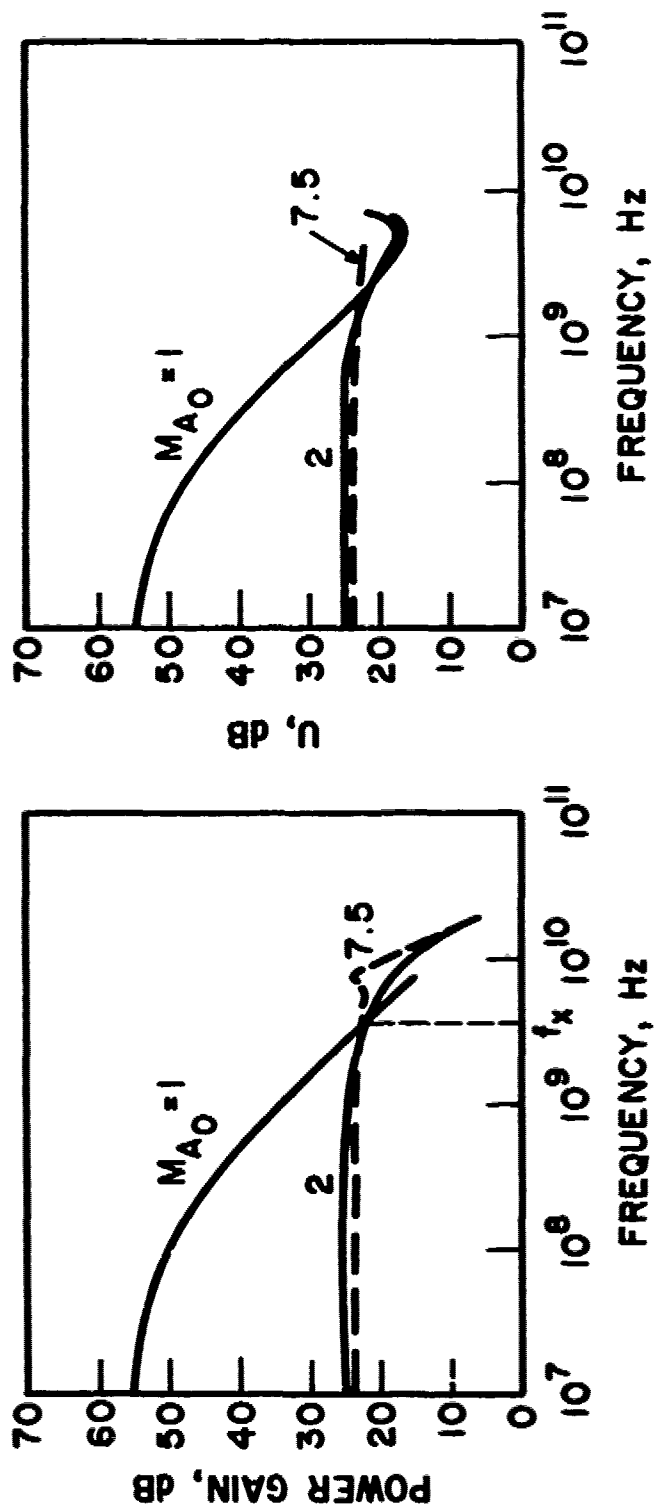
FIG. 3.11 MAXIMUM RF POWER GAIN AND U VS. FREQUENCY. ($w_T = 4 \times 10^{-4}$ cm AND $V_{EB_O} = 0.7$ V)
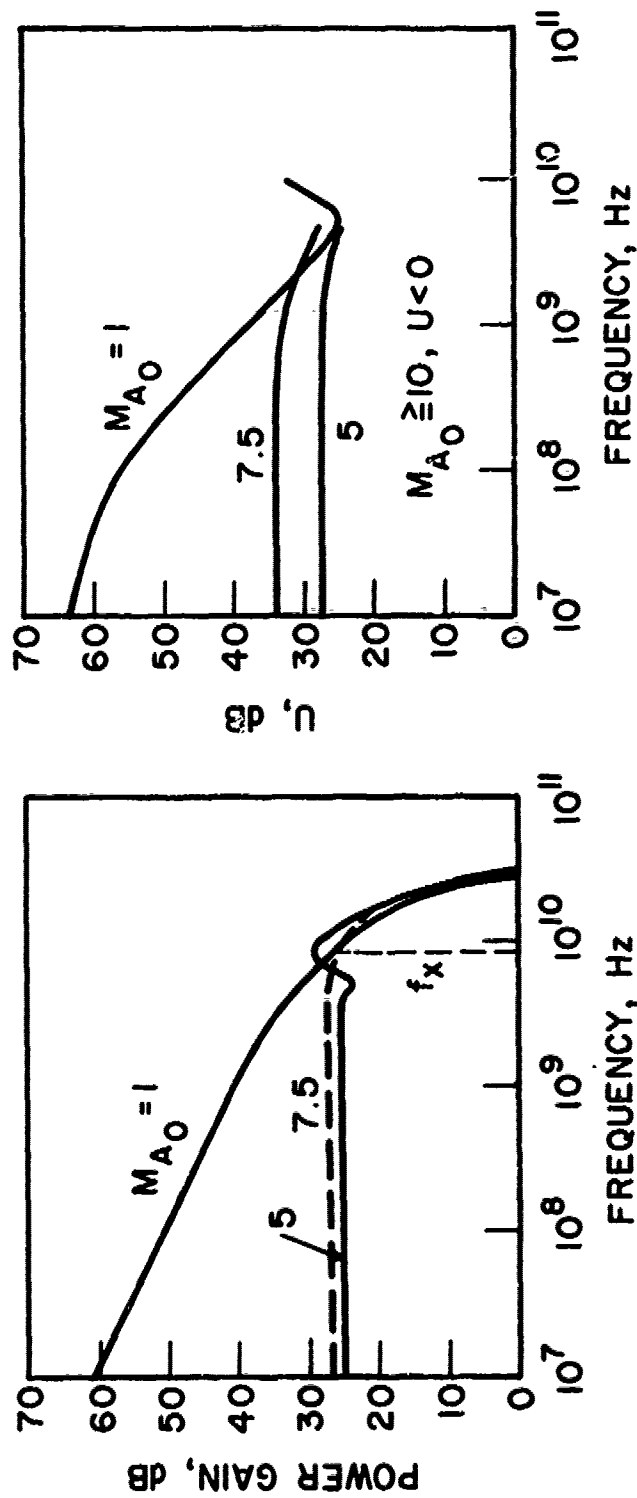
FIG. 3.12 MAXIMUM OPERATING POWER GAIN AND U VS. FREQUENCY. $(w_T = 4 \times 10^{-4}$ cm AND $V_{EB_o} = 0.8$ V)
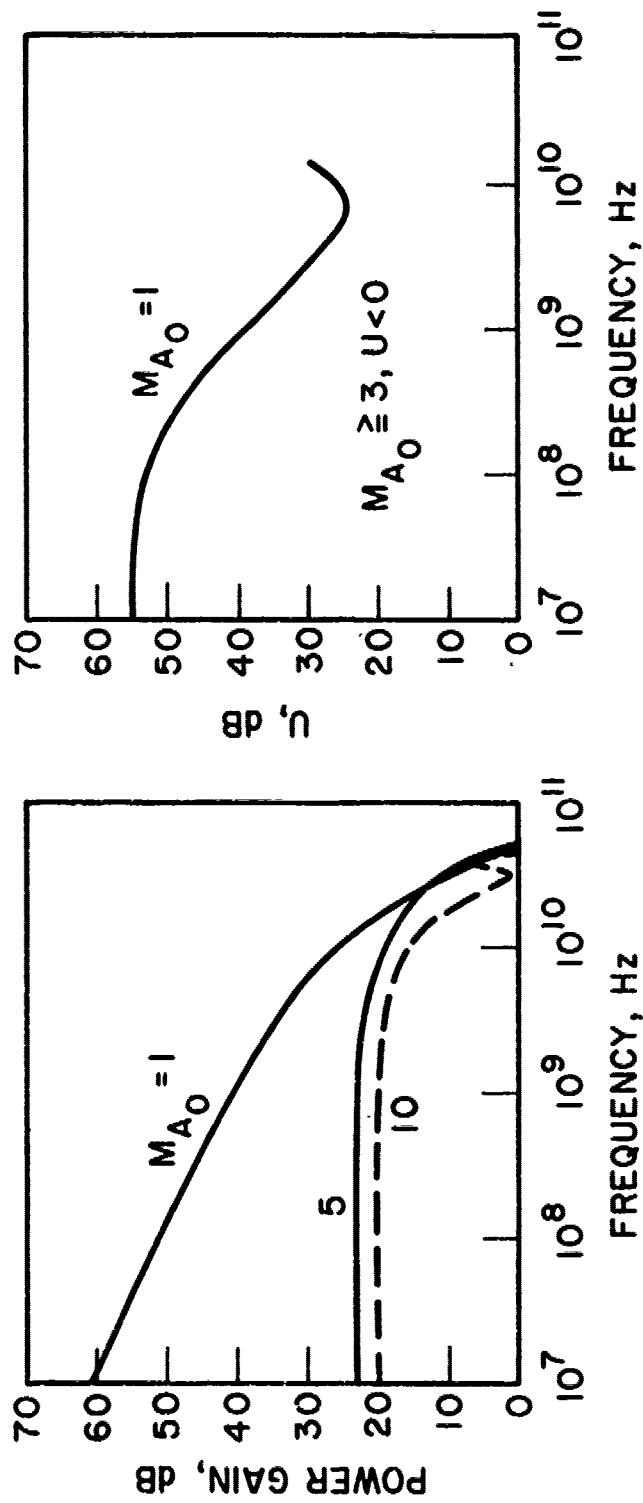
FIG. 3.13 MAXIMUM RF POWER GAIN AND U VS. FREQUENCY. ($w_T = 4 \times 10^{-4}$ cm AND $V_{EB_o} = 0.85$ V)
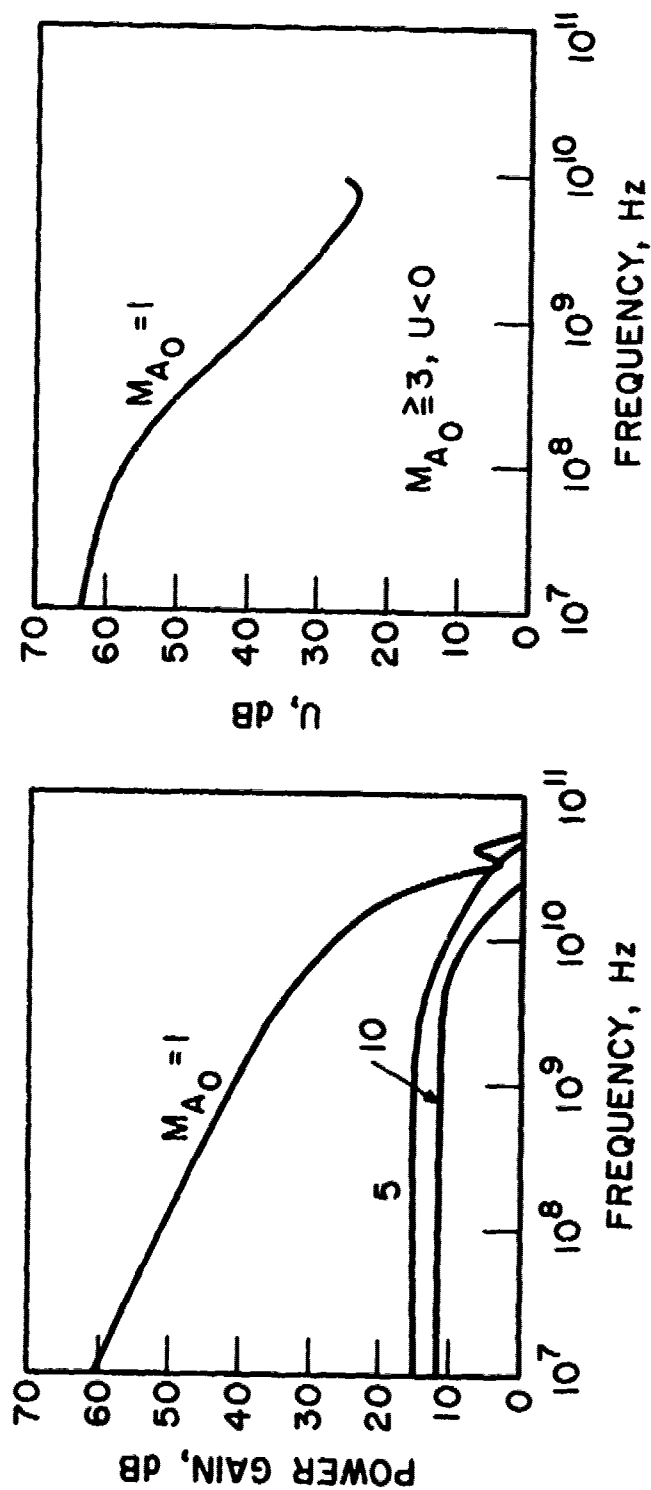
FIG. 3.14 MAXIMUM OPERATING POWER GAIN AND U VS. FREQUENCY. ($w_T = 4 \times 10^{-4}$ cm AND $V_{EB_o} = 0.9$ v)

gain greater than unity occurs. From Figs. 3.11 and 3.12 it is

observed that at frequencies higher than f_x, avalanche multiplication

also increases the operating power gain. IF $V_{EB_o} > 0.85$ V, f_{max}

decreases with increasing M_{A_o} and the operating power gain at $M_{A_o} > 1$

is smaller than the operating power gain at $M_{A_o} = 1$ throughout the entire

active frequency range. The effects of V_{EB_o} on f_{max} and the operating

power gain are illustrated in Fig. 3.15. Highest f_{max} at $M_{A_o} = 5$ is

achieved when $V_{EB_o} = 0.7$ V. Highest operating power gain at $M_{A_o} = 5$ is

achieved when $V_{EB_o} = 0.8$ V. When $V_{EB_o} \lesssim 0.7$ V, f_{max} is severely limited

by a large value of the emitter space-charge resistance. When $V_{EB_o} \gtrsim$

0.85 V, f_{max} and operating power gain are reduced due to large values of

$J_{nB_{dc}}$. From Eq. 3.45, there are two components in J_{T_1}. One component

represents the carriers contained in J_{nB_1} undergoing constant avalanche

multiplication which is determined by V_{T_o}. The second component, which

is

$$\frac{A_E\left(J_{nB_{dc}} + J_{c_{ns}} + J_{c_{ps}}\right)\left(M_{A_o} - 1\right)\left[\ln(w_{av}A) - \ln\left(1 - \frac{1}{M_{A_o}}\right)\right]^2}{\left(\frac{1}{M_{A_o}} + j\,\frac{\omega\tau_g}{2}\right)(bw_T)}$$

$$\cdot\,\frac{\sin\frac{\theta_D}{2}}{\frac{\theta_D}{2}}\,e^{-j(\theta_D/2)}\,V_{T_1}\,,$$

represents the carriers corresponding to $J_{nB_{dc}} + J_{c_{ns}} + J_{c_{ps}}$ undergoing

nonconstant avalanche multiplication which depends on the instantaneous

voltage $V_T = V_{T_o} + V_{T_1}\,e^{j\omega t}$. The second current component is

responsible for the decreases in f_{max} and the operating power gain as
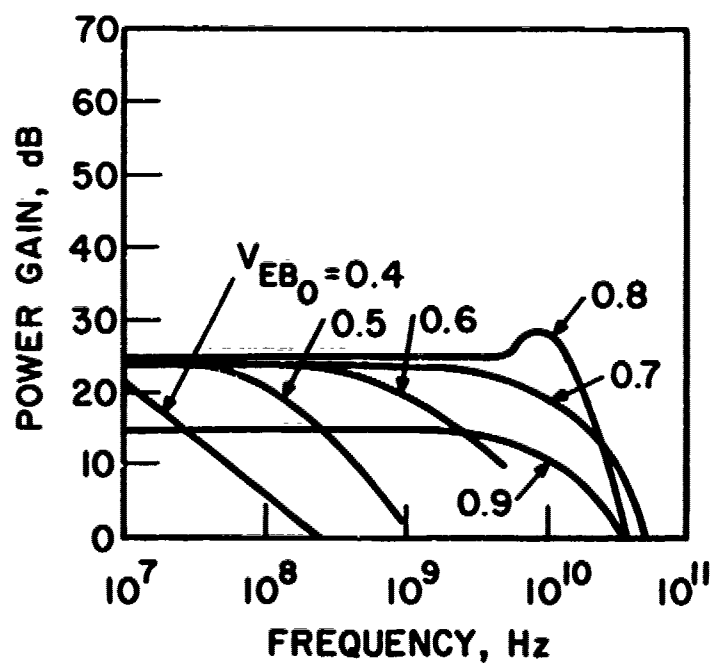
FIG. 3.15   MAXIMUM OPERATING POWER GAIN VS. FREQUENCY.

$(w_T = 4 \times 10^{-4}$ cm AND $M_{A_O} = 5)$

M_{A_o} increases. If the second current component is artificially forced

to vanish, the corresponding maximum operating power gain and U are

displayed in Figs. 3.16 and 3.17. Note that the power gain and f_{max}

at M_{A_o} = x are always less or equal to operating power gain and f_{max}

at M_{A_o} = y, if x < y. Figure 3.18 shows that for a given value of M_{A_o},

higher V_{EB}, up to 0.8 V, implies higher f_{max} and higher operating power

gain. For V_{EB_o} > 0.8 V, maximum operating power gain coincides with

that corresponding to V_{EB_o} = 0.8 V. Comparison of previous results and

the results obtained by artificially setting the second current component

to zero indicates that, for the most part, avalanche multiplication of

carriers in CATT amplifiers, when operating in Class A, works toward

reducing the operating power gain. The situation is that the value of

V_{EB_o} must not be too small, otherwise, the emitter space-charge resistance

will severely reduce f_{max} and the operating power gain, and if the value

of V_{EB_o} is large, the second current component will dominate which has

been shown to degrade the operating power gain. From the expression

for I_{T_1}, the phase difference between V_{T_1} and the second current component

equals $(\theta_D/2) + \tan^{-1}(\omega \tau_g M_{A_o}/2)$. If $-\pi/2$ < phase difference < $\pi/2$, energy

is being dissipated. The situation in Class A operation at low frequency

is depicted in Fig. 3.19. It is assumed that the load is a high-Q

tank circuit whose resonant frequency equals the emitter-base input

signal frequency. Notice that the amplitude of the first current

component, when V_{T_1} is large, is less than the value given by Eq. 3.45.

The reason for this is that when I_{nB_1} is maximum, V_T is minimum and the

carrier multiplication is at its minimum. When I_{nB_1} is minimum, V_T

is maximum and the carrier multiplication is at its maximum. This
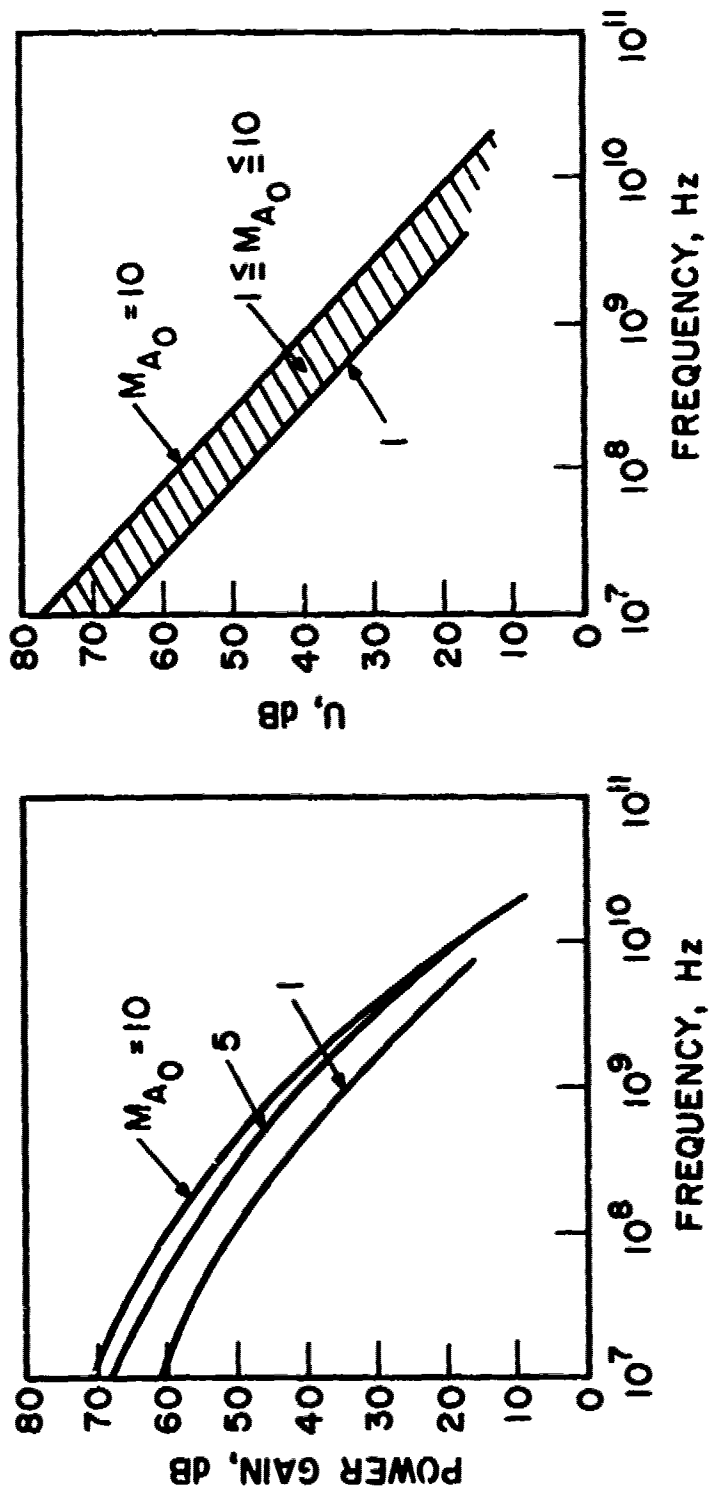
FIG. 3.16 MAXIMUM OPERATING POWER GAIN AND U VS. FREQUENCY WHEN AVALANCHE MULTIPLICATION

OF CARRIERS CORRESPONDING TO $J_{nB_{dc}}$ IS IGNORED. ($w_T = 4 \times 10^{-4}$ cm AND $V_{EB_o} = 0.7$ V)
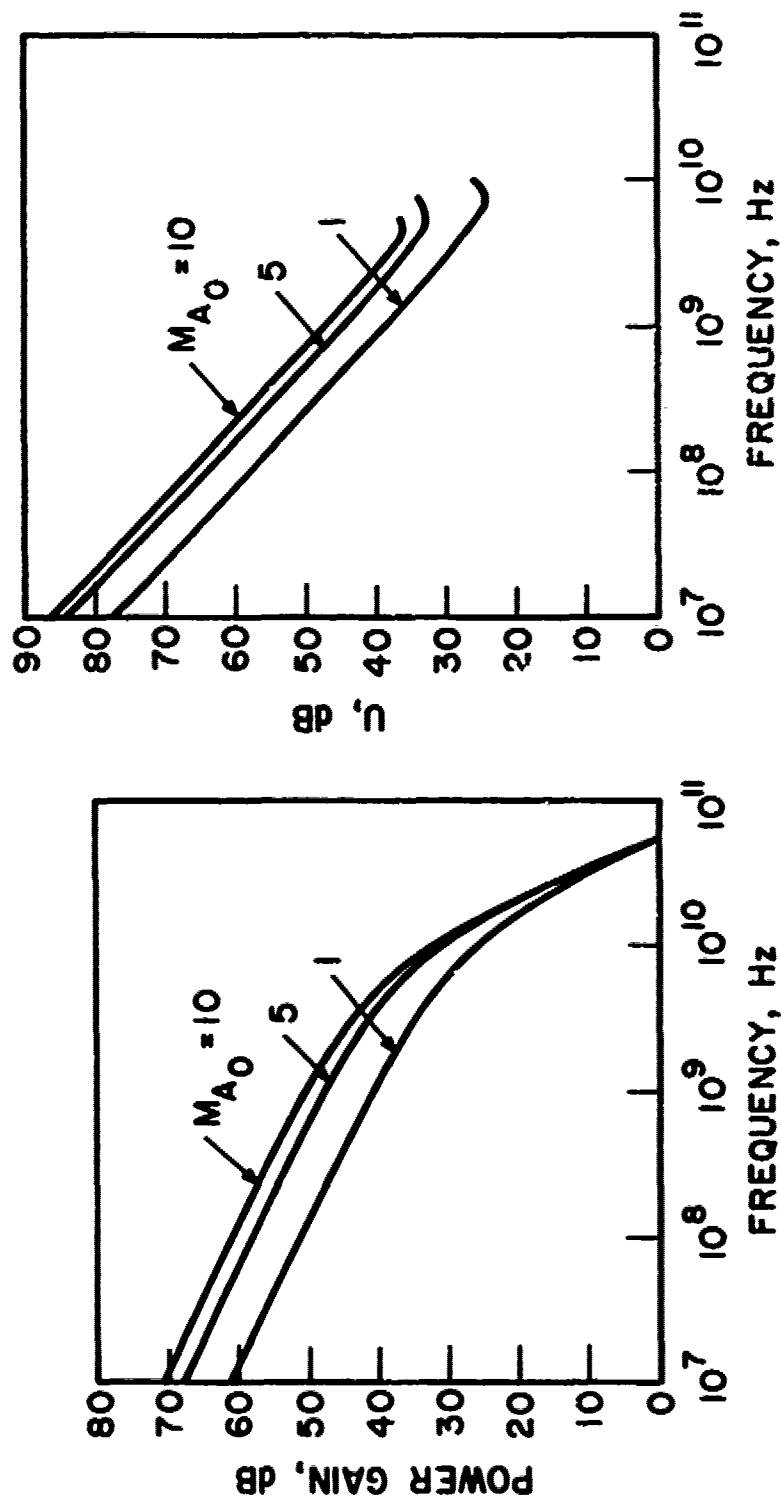
FIG. 3.17 MAXIMUM OPERATING POWER GAIN AND U VS. FREQUENCY WHEN AVALANCHE MULTIPLICATION

OF CARRIERS CORRESPONDING TO $J_{nB_{dc}}$ IS IGNORED. ($w_T = 4 \times 10^{-4}$ cm AND $V_{EB_o} = 0.85$ V)
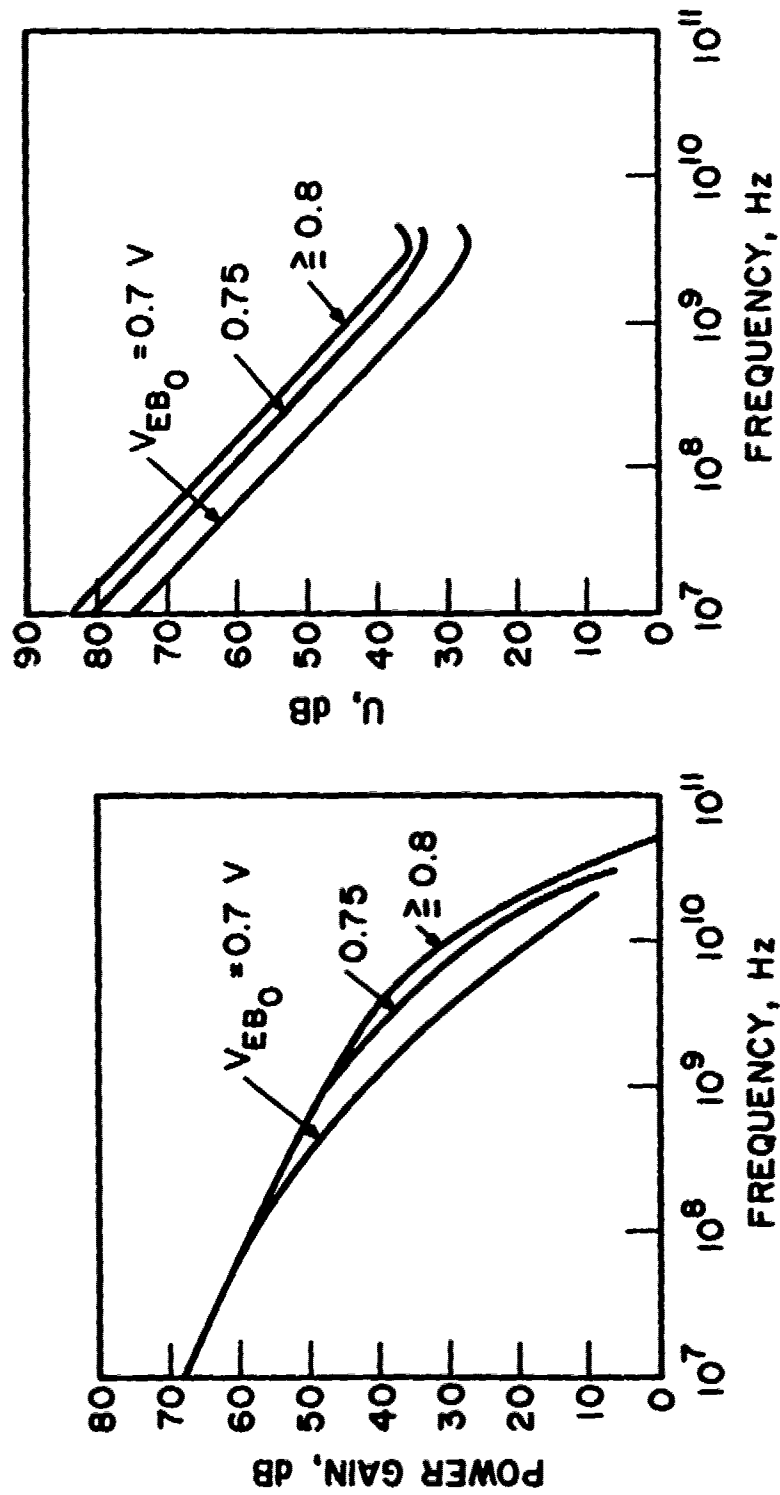
FIG. 3.18 MAXIMUM OPERATING POWER GAIN AND U VS. FREQUENCY WHEN AVALANCHE MULTIPLICATION

OF CARRIERS CORRESPONDING TO $J_{nB_{dc}}$ IS IGNORED. ($w_T = 4 \times 10^{-4}$ cm AND $M_{A_o} = 5$)
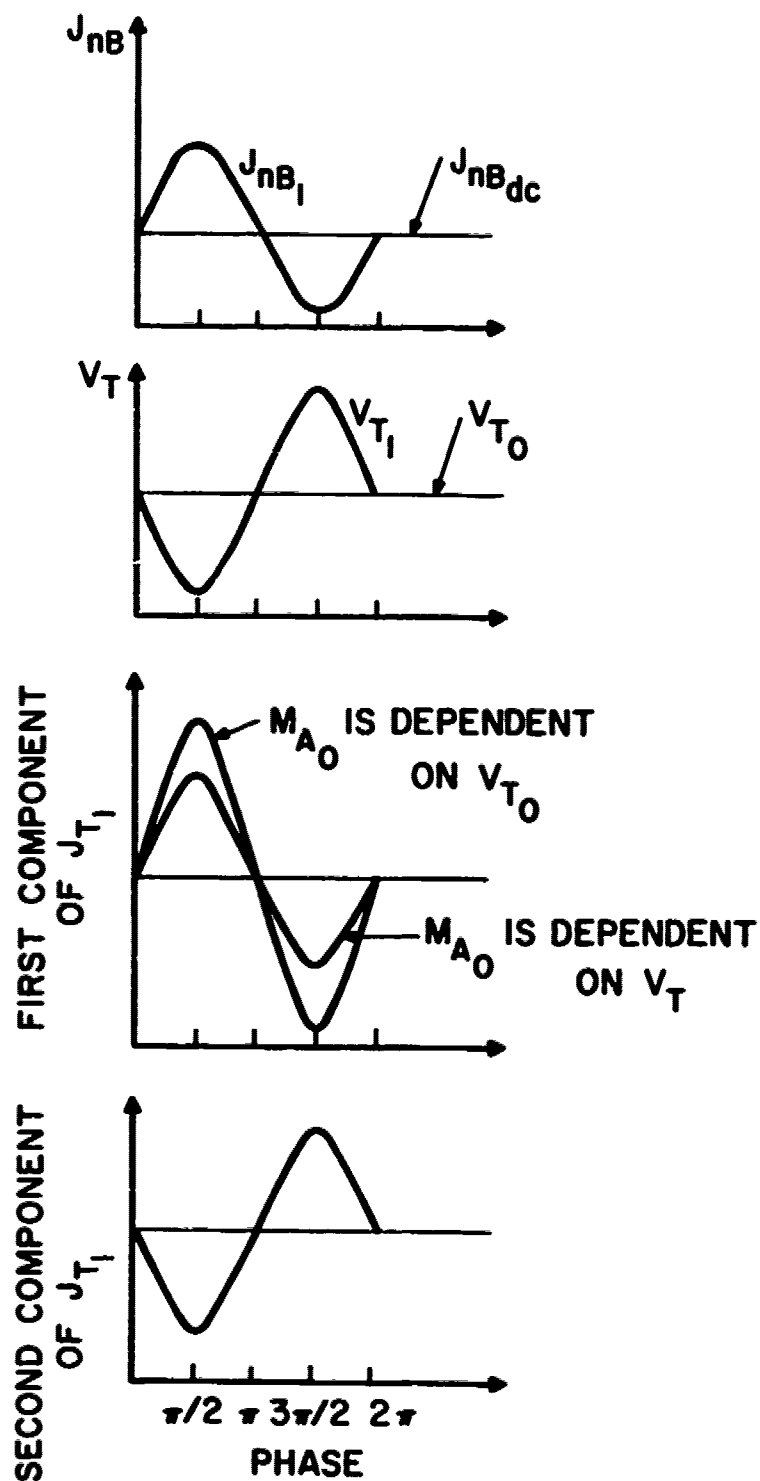
FIG. 3.19 SCHEMATIC PLOTS OF J_{nB}, V_T, FIRST COMPONENT OF J_{T_1}, AND SECOND COMPONENT OF J_{T_1}.

situation can be seen by following the load line in Fig. 3.10. From the phase relationship between V_{T_1} and the second current component, it is clear that the second current component corresponds to energy dissipation, therefore, it reduces the operating power gain. The usefulness of carrier multiplication and long transit region can be realized only in Class C operation, assuming a proper load is applied across the base-collector terminal and the width of the charge pulse is much less than π rad. The Class C operation of CATT amplifiers was briefly described in Chapter I and the large-signal simulation results are discussed in detail in Chapter IV.

3.5 Operation of a CATT as an IMPATT with Variable Equivalent Thermally Generated Current

There has been considerable interest in the operation of an IMPATT diode with an externally controllable equivalent thermally generated current. Sanderson and Jordan[56] discussed the operation of an IMPATT acted upon by an electron beam. The electron-beam-produced current is subject to multiplication in the same way as the flow of actually thermally generated carriers. The sum of the electron-beam-produced current and the current due to thermally generated carriers is, by definition, the equivalent thermally generated current. Sanderson and Jordan derived small-signal IMPATT expressions which theoretically predict that an appreciable change in the IMPATT resonant frequency can be induced by varying the electron-beam intensity. Results suggest that frequency modulation of the IMPATT oscillator can be implemented by this method. Forrest and Seeds[57] and others have studied the controlling of microwave IMPATT oscillators with an optical signal.

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The use of an electron beam or an optical signal on an IMPATT
is equivalent to the situation where the base collector of a CATT is
operated as an IMPATT where the emitter and base simply act as an
externally controlled thermal current source. The expressions derived
by Sanderson and Jordan can simply be obtained from Eqs. 3.37 by
allowing $M_{A_o} \to \infty$ and $J_{nB}(t) = J_{nB_{dc}}$.

3.6 Conclusions

In this chapter analytical expressions required for dc and ac
small-signal CATT device models have been derived. A simple computer
program, DCCP, has been written which can generate the common-base
characteristics of various CATT devices at minimal cost. Another
computer program, SSCP, has been developed which can find the device
small-signal y-parameters, unilateral gain, maximum operating power gain,
optimum load, inherent input and output bandwidth, Linvill stability
factor, amplifier tunability, and the maximum frequency of oscillation.
The output results of SSCP indicate that under certain restricted
operating conditions f_{max} increases with increasing M_{A_o} and the
operating power gain at $M_{A_o} > 1$ is higher than the operating power gain
at $M_{A_o} = 1$ for frequencies higher than a critical value f_x. However,
for frequencies lower than f_x, the operating power gain at $M_{A_o} = 1$ is
always much higher than the operating power gain at $M_{A_o} > 1$. The cause
for the gain reduction was determined to be the component of J_{T_1} due
to V_{T_1}-dependent multiplication of those carriers corresponding to $J_{nB_{dc}}$.
This component of J_{T_1} represents energy dissipation. Computational
results of SSCP and DCCP indicate that Class A operation is not very
suitable for CATT amplifiers.

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CHAPTER IV.   LARGE-SIGNAL COMPUTER MODEL

4.1 Introduction

In this chapter a large-signal computer simulation is developed
which is hybrid in the sense that the emitter and base regions are
modeled by lumped, nonlinear and time-varying circuit elements whose
values are determined by a set of analytical expressions while the
collector region is modeled by employing the difference-equations
version of the semiconductor differential equations. The analytical
expressions for the circuit elements of the lumped-circuit model for
the emitter and base regions are derived. The numerical methods used
to solve the difference equations are modified versions of techniques
which have evolved in the Electron Physics Laboratory in the past
decade.[58-62] Detailed descriptions of the numerical algorithms,
computer programs, and computer output are also given.

4.2 Development of Device Simulation

4.2.1 General Description.

Figure 3.1 shows the depletion
regions of a normally biased CATT device and its circuit model is shown
in Fig. 4.1. The emitter-base region of the CATT device is represented
by three nonlinear circuit elements similar to those in BJTs: a diode
in which the particle current is injected across the forward-biased
emitter-base junction whose magnitude depends on the emitter-base
junction voltage V_{EBJ}, a V_{EBJ}-dependent depletion capacitance C_{TE},
and a V_{EBJ}-dependent diffusion capacitance C_{DE}. Resistor R_B is the
equivalent base region spreading resistance. The collector region is
represented by a capacitor C_c and a dependent current source I_T. The

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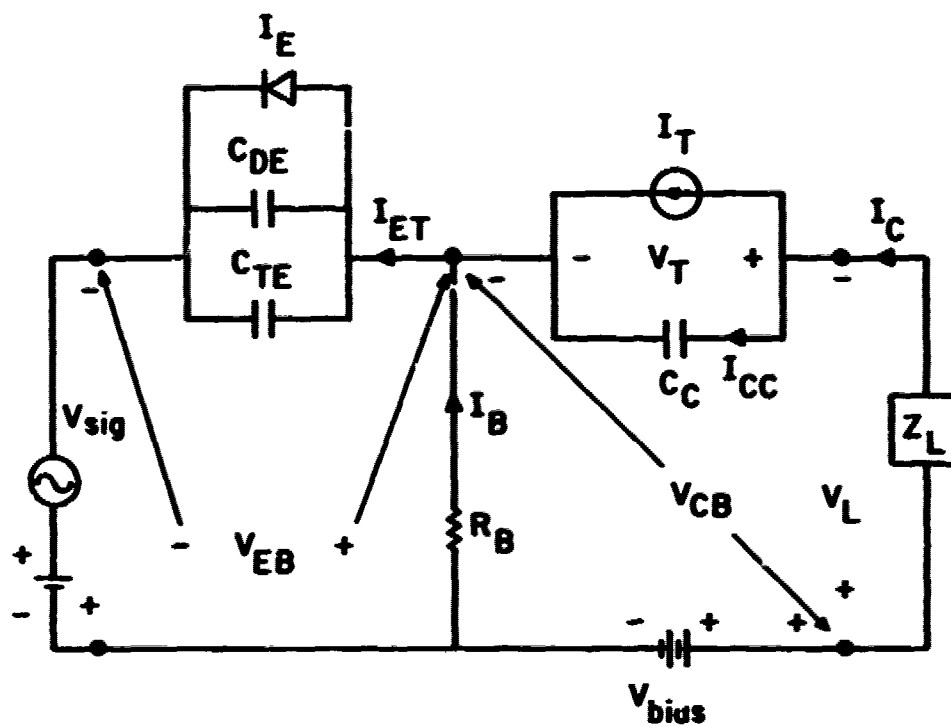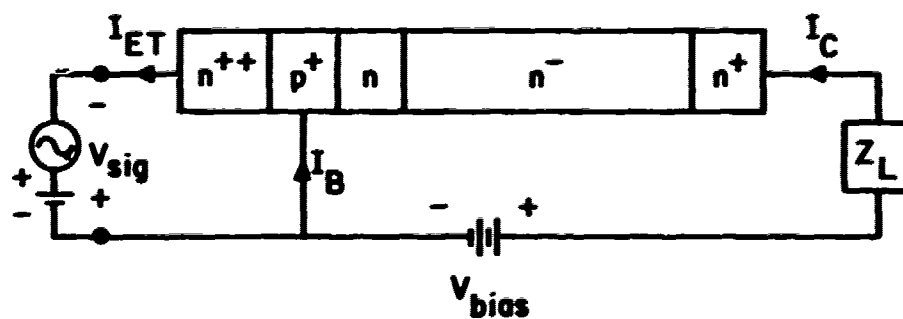
FIG. 4.1 CIRCUIT MODEL FOR A CATT AMPLIFIER IN THE

COMMON-BASE CONFIGURATION.

capacitor C_c is the collector depletion capacitance and the dependent current source I_T represents the induced current whose value depends on the amount of charge injected into the depleted collector region from the neutral base region and the magnitude of carrier multiplication. It is assumed that the drift region is always completely or nearly completely depleted. Otherwise a V_T-dependent resistor must be added in series with the collector circuit representation depicted in Fig. 4.1. The remainder of this section is devoted to detailed derivation and physical interpretation of each element of the device model.

$\underline{4.2.2}$ $\underline{\text{Emitter-Base}}$ $\underline{\text{Circuit}}$ $\underline{\text{Model}}$ $\underline{\text{and}}$ $\underline{\text{Computer}}$ $\underline{\text{Program}}$ $\underline{\text{EBCP}}$. In the bulk of the base region, the space-charge neutrality condition always holds. Thus in the base region of n-type CATT devices,

$$n(y) + N_A(y) - p(y) = 0 \quad . \tag{4.1}$$

An important observation about current in n-type CATT devices is that there is a negligible flow of holes (majority carriers) in most of the base region between the emitter-base and base-collector metallurgical junctions in the reverse direction. This is true under all bias conditions because there can be only a vanishingly small flow of holes from either n-region. The following expressions can be written for hole current in the longitudinal dimension y and the electric field:

$$J_p = 0 = e\mu_p p E(y) - eD_p \frac{dp}{dy}$$

and

$$E(y) = \frac{kT}{e} \frac{1}{p} \frac{dp}{dy} \quad , \tag{4.2}$$

where p, the concentration of holes in the bulk base region, is related to n and N_A through Eq. 4.1. In a uniformly doped base region, the electric field is negligible at low injection levels, that is, when the concentration of minority carriers is much lower than the base region impurity doping concentration. Therefore, the emitter-base junction voltage V_{EBj} equals the emitter-base terminal voltage V_{EB}. At high injection levels, the electron concentration is significantly higher than its thermal equilibrium concentration and the electric field in the bulk base region can no longer be ignored. A portion of the emitter-base terminal voltage appears across the neutral base region such that V_{EBj} is less than V_{EB}:

$$V_{EBj} = V_{EB} - \int_{w_2}^{w_3} E(y) \, dy \quad .$$

By substituting the expression in Eq. 4.2 into the preceding relation, V_{EBj} can be expressed as follows:

$$V_{EBj} = V_{EB} - \frac{kT}{e} \ln\left[\frac{p(w_2)}{N_A}\right] \quad . \tag{4.3}$$

By using Eq. 4.3; the charge neutrality condition at $y = w_2$; and the junction law, $n(w_2) = n_o(w_2) \exp (eV_{EBj}/kT)$, the following expression for V_{EBj} is derived:

$$V_{EBj} = V_{EB} - \frac{kT}{e} \ln\left[\frac{1}{2}\left(1 + \sqrt{1 + \frac{4n_i^2 \exp (eV_{EB}/kT)}{N_A^2}}\right)\right] \quad , \tag{4.4}$$

where n_i is the intrinsic carrier concentration. In order to be

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assured that Eq. 4.4 is valid at any injection level, it is necessary to prove first that the junction law is valid at any injection level.

Figure 4.2 shows the space-charge distribution and the voltage distribution $\psi(y)$ in the depletion region of a p-n step junction where a voltage - V is applied to the n-region. In the space-charge region of a p-n junction there is a large field strength E and a large carrier density gradient. In the current density equation for holes,

$$J_p = e\mu_p pE - eD_p \frac{dp}{dy} \quad ,$$

the current density J_p is the difference between two large opposing currents so that $|J_p| \ll e\mu_p p|E|$ and $|J_p| \ll eD_p|dp/dy|$ for most of the space-charge region. Hence a good approximation is

$$- e\mu_p p \frac{d\psi}{dy} - eD_p \frac{dp}{dy} \simeq 0$$

or

$$p(y) = p(w_2) \exp[- e\psi(y)/kT] \tag{4.5}$$

for $- w_1 \overset{\le}{=} y \overset{\le}{=} w_2$. Similarly, for electrons the following is obtained

$$n(y) = n(- w_1) \exp\left[- \frac{e[V_{BI} - V_{EBj} - \psi(y)]}{kT}\right] \tag{4.6}$$

for $- w_1 \overset{\le}{=} y \overset{\le}{=} w_2$ where V_{BI} is the junction built-in potential. Here it is assumed that the quasi-Fermi levels for electrons and holes are constant in the depletion region. By using Eqs. 4.1, 4.5 and 4.6, the following expressions are obtained:
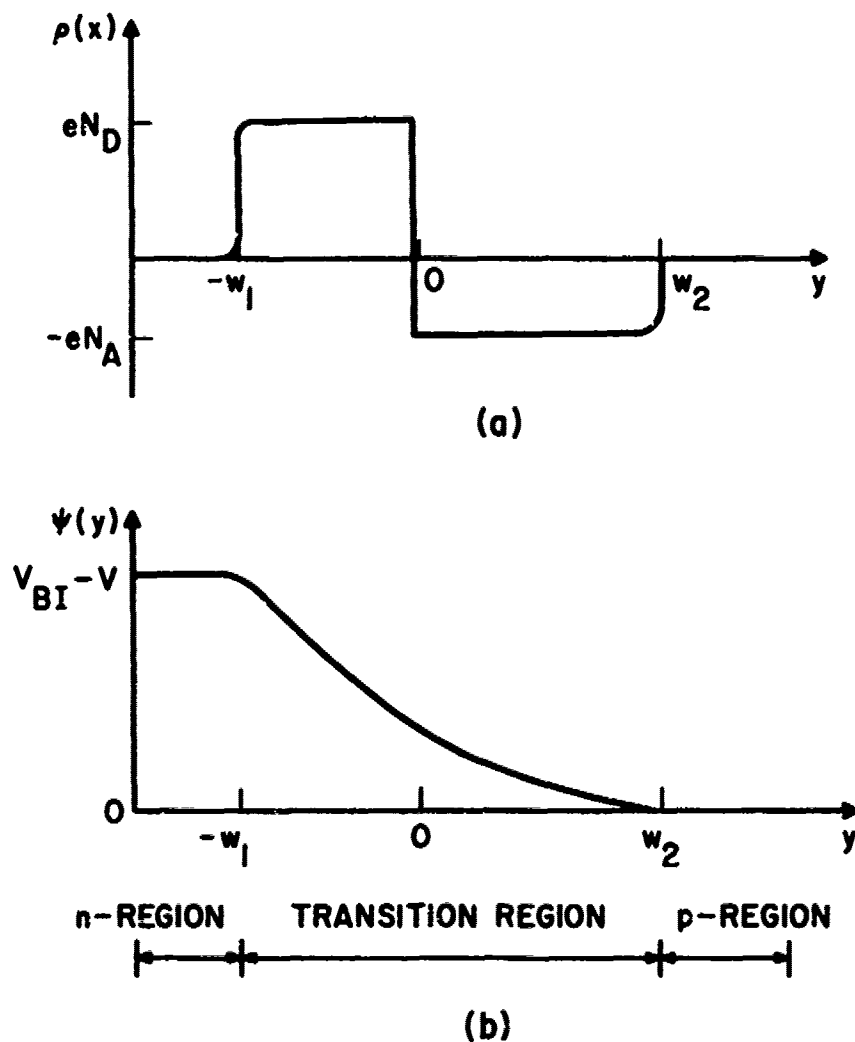
FIG. 4.2 (a) SPACE-CHARGE DISTRIBUTION IN A p-n STEP JUNCTION

AND (b) VOLTAGE DISTRIBUTION IN A p-n JUNCTION; A

VOLTAGE - V IS APPLIED TO THE n-REGION. V_{BI} IS THE

JUNCTION BUILT-IN POTENTIAL.

$$p(-w_1) = \frac{N_A B + N_D B^2}{1 - B^2} \quad , \qquad (4.7)$$

$$n(-w_1) = \frac{N_A B + N_D}{1 - B^2} \quad , \qquad (4.8)$$

$$p(w_2) = \frac{N_A + N_D B}{1 - B^2} \qquad (4.9)$$

and

$$n(w_2) = \frac{N_A B^2 + N_D B}{1 - B^2} \quad , \qquad (4.10)$$

where

$$B = \exp\left[-e(V_{BI} - V_{EBj})/kT\right] \quad .$$

Based on the facts that in n-type CATT devices $N_D \gg N_A$ and B is generally much less than one, Eqs. 4.8 and 4.10 can be reduced to

$$n(-w_1) \simeq N_D$$

and

$$n(w_2) \cong N_D B$$

$$= n_o(w_2) \exp(eV_{EBj}/kT) \qquad (4.11)$$

and they are always valid regardless of the injection level. On the other hand, Eqs. 4.7 and 4.9 are reduced to

$$p(-w_1) \cong N_A B$$

$$= p_o(-w_1) \exp\left(eV_{EBj}/kT\right)$$

and

$$p(w_2) = N_A$$

if $N_A/N_D \gg B$, which is the low injection level condition. When the injection level is no longer restricted to low injection levels, hole concentrations at $y = -w_1$ and w_2 are given by

$$p(-w_1) = \{p_o(-w_1) + n_o(w_2) \exp\left[-e(V_{BI} - V_{EBj})/kT\right]\}$$

$$\cdot \exp(eV_{EBj}/kT)$$

and

$$p(w_2) = N_A + n(w_2) \ .$$

It has been shown that the junction law for electrons is always valid in an n-type CATT device in which $N_D \gg N_A$ and therefore Eq. 4.4 is valid at any injection level.

It has been shown that, except at low injection levels, there is a finite voltage drop in the bulk base region and there exists a finite electric field. This electric field aids the flow of minority carriers in the bulk base region. An effective diffusion constant can be defined which includes the effect of the drift field. The expression for the electron current density is

$$J_n = e\mu_n nE + eD_n \frac{dn}{dy} \ .$$

Substituting the relation in Eq. 4.2 into the preceding expression yields

$$J_n = eD_n\left(1 + \frac{n}{N_A + n}\right)\frac{dn}{dy} \quad ,$$

and when it is evaluated at $y = w_2$, the result is

$$J_{nE} = \frac{eD_n}{w_B}\left[1 + \frac{1}{1 + \frac{N_A}{n_o(w_2)\exp(eV_{EBj}/kT)}}\right] n_o(w_2)[\exp(eV_{EBj}/kT) - 1] \quad ,$$

where

$$w_B = w_3 - w_2 \quad .$$

At low injection levels, the expression for J_{nE} is

$$J_{nE} = \frac{eD_n}{w_B} n_o(w_2)[\exp(eV_{EB}/kT) - 1] \quad ,$$

and at very high injection levels the expression for J_{nE} becomes

$$J_{nE} = \frac{2eD_n}{w_B} n_o(w_2)\exp(eV_{EBj}/kT) \quad .$$

The following can then be written:

$$I_{nE} = \frac{eA_E D_{nEFF}}{w_B}[n(w_2) - n_o(w_2)] \quad , \tag{4.12}$$

where

$$D_{nEFF} = D_n\left(1 + \frac{1}{1 + \frac{N_A}{n(w_2)}}\right) \quad .$$

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Depletion region widths w_1, w_2 and w_3 can be calculated by using the following analytical expressions:

$$w_1 = \left(\frac{2\epsilon}{eN_D}\right)\left[\frac{N_A}{N_A + N_D}\right]^{1/2} \frac{1}{\sqrt{V_{BI} - V_{EBj}}} \ , \qquad (4.13)$$

$$w_2 = \left(\frac{2\epsilon}{eN_A}\right)\left[\frac{N_D}{N_A + N_D}\right]^{1/2} \frac{1}{\sqrt{V_{BI} - V_{EBj}}} \qquad (4.14)$$

and

$$w_3 \cong w_{B_0} - \frac{\epsilon E(w_{B_0})}{eN_A} \ , \qquad (4.15)$$

where V_{EBj} is calculated by using Eq. 4.4 and $E(w_{B_0})$ is provided by the collector simulation computer program CCP which is discussed in Section 4.2.3. The Early effect[3] of base width modulation is included in this device model through Eqs. 4.14 and 4.15.

An expression for the emitter particle current, which is valid at any injection level, can be obtained from Eq. 3.14 by replacing D_n, $n(w_2)$, $p(-w_1)$, V_{EB}, and w_{B_0} with the appropriate expressions that have been derived in this section. The emitter particle current is given by

$$I_E = eA_E\left\{\frac{D_{nEFF}}{w_B}\left[n(w_2) - n_0(w_2)\right] + \frac{D_p}{w_E}\left[p(-w_1) - p_0(-w_1)\right]\right\} \ , \quad (4.16)$$

where

$$w_E = w_{E_o} - w_1 \quad \text{if} \quad w_{E_o} - w_1 < L_p$$

and

$$w_E = L_p \quad \text{if} \quad w_{E_o} - w_1 > L_p \ .$$

The charge Q_{EB} on each side of the emitter-base junction is

$$Q_{EB} = eN_D w_1 = eN_A w_2 \ .$$

Using the preceding relations yields

$$C_{TE} = \frac{dQ_{EB}}{d(V_{BI} - V_{EBj})}$$

$$= \frac{A_E}{2} \left[2e\epsilon \ \frac{N_D N_A}{N_D + N_A} \right]^{1/2} (V_{BI} - V_{EBj})^{-(1/2)} \ . \tag{4.17}$$

The displacement current through C_{TE} is I_{CTE} and is given by

$$I_{CTE} = \frac{dQ_{EB}}{dV_{EBj}} \ \frac{dV_{EBj}}{dt}$$

$$= C_{TE} \ \frac{dV_{EBj}}{dt}$$

$$= C_{TE} \ \frac{dV_{EB}}{dt} \ . \tag{4.18}$$

The emitter-base diffusion capacitance C_{DE} is associated with the storage of minority carriers in the bulk base region. If straight-line minority carrier distribution and $n(w_3) = 0$ are assumed, the total minority carrier charge stored in the neutral base region is

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$$Q_B = \frac{1}{2} e A_E w_B n_o(w_2) \exp{(eV_{EBj}/kT)} \quad ,$$

and the current associated with C_{DE} is

$$I_{CDE} = \frac{dQ_B}{dt}$$

$$= \frac{dQ_B}{dV_{EBj}} \frac{dV_{EBj}}{dt}$$

$$\approx C_{DE} \frac{dV_{EB}}{dt} \quad , \tag{4.19}$$

where

$$C_{DE} = \frac{dQ_B}{dV_{EBj}}$$

$$= \frac{e}{kT} I_{nE} \frac{w_B^2}{2D_{nEFF}} \quad . \tag{4.20}$$

In reality $n(w_3)$ cannot be zero[63] because nonzero electron current density exists at $y = w_3$. Because of nonzero $n(w_3)$, an additional charge will be stored in the base. Kirk[51] showed that the fluctuation of this stored charge in response to the input signal will introduce an additional time delay, approximately equal to w_B/v_{ns}, where v_{ns} is the electron saturated velocity. There is another time delay which is associated with emitter heavy doping. Until recently[64-66] it had been assumed that the emitter should be as heavily doped as possible in order to ensure a high emitter injection efficiency. However, high doping will lead to the formation of band-edge tails and impurity level

broadening[64,67] into an impurity band. DeMan[54] introduced a doping-dependent intrinsic carrier concentration n_i to account for the effect of heavy doping on the classical expressions for the electrical parameters. The validity of this approach was later verified theoretically.[65,67] Under heavy doping conditions the hole current density injected into the emitter from the base is given by[68]

$$J_p = eD_p \left[\frac{p}{n_i^2} \frac{dn_i^2}{dy} - \frac{p}{N_D} \frac{dN_D}{dy} - \frac{dp}{dy} \right] .$$

The holes experience an additional drift force proportional to the derivative of the change of the valence band edge. Therefore an additional component of hole current flowing from the base into the emitter of an n-type CATT device is introduced. Additional holes stored in the emitter cause an emitter delay time given by

$$\tau_e = \frac{1}{\beta_o} \int_0^{w_{E_o} - w_1} \frac{n_i^2}{N_D} \left(\int_0^y \frac{N_D}{D_p n_i^2} \, dy \right) dy ,$$

where $\beta_o \triangleq (D_n N_D w_{E_o} / D_p N_A w_{B_o})$. Therefore, microwave CATT devices are designed to have narrow emitter junction depths not only to reduce the emitter capacitance and the emitter sidewall capacitance, but also to reduce τ_e. Henderson and Scarbrough[69] considered the special case of flat arsenic and boron concentrations in the emitter region. In this case N_D and n_i are both constant and therefore τ_e is given by

$$\tau_e = \frac{w_{E_o}^2}{2D_p \beta_o^2} .$$

By including the two additional time delays, an effective diffusion capacitance can be defined as follows:

$$C_{DEFF} = \frac{e}{kT} I_{nE}\left(\frac{w_B^2}{2.43D_{nEFF}} + \frac{w_E}{v_{ns}} + \frac{w_{E_o}^2}{2D_p\beta_o^2}\right) . \qquad (4.21)$$

The base spreading resistance is calculated by using Eq. 3.19 and for convenience it is stated again below:

$$R_B = \left(\underbrace{\frac{w}{12x_B\,\sigma_B\ell}}_{1} + \underbrace{\frac{d}{2x_B\,\sigma_B\ell}}_{2}\right) \frac{1}{\text{number of emitter-base finger pairs}} ,$$

where the device structure is defined in Fig. 3.2. Base region conductivity modulation due to electron and hole carriers and the base region width modulation due to the Early effect are ignored in Eq. 3.19 although these effects can easily be included in the analysis.

The computer program for the emitter-base region EBCP solves the circuit model in Fig. 4.3. It is assumed that V_{sig}, R_B, and I_c, the total collector current, are known quantities where the current I_c is provided by the collector computer program CCP. Kirchhoff's voltage law demands

$$V_{sig}(t) - V_{EB}(t) - R_B\left(I_E(V_{EB}) + [C_{TE}(V_{EB}) + C_{DE}(V_{EB})]\,\frac{dV_{EB}}{dt}\right.$$
$$\left. - I_c(t)\right) = 0 .$$

This equation can be written as

$$\frac{dV_{EB}(t)}{dt} = \frac{1}{C_{TE}(V_{EB}) + C_{DE}(V_{EB})}\left(\frac{1}{R_B}\,[V_{sig}(t) - V_{EB}(t)]\right.$$
$$\left. + I_c - I_E(V_{EB})\right) , \qquad (4.22)$$

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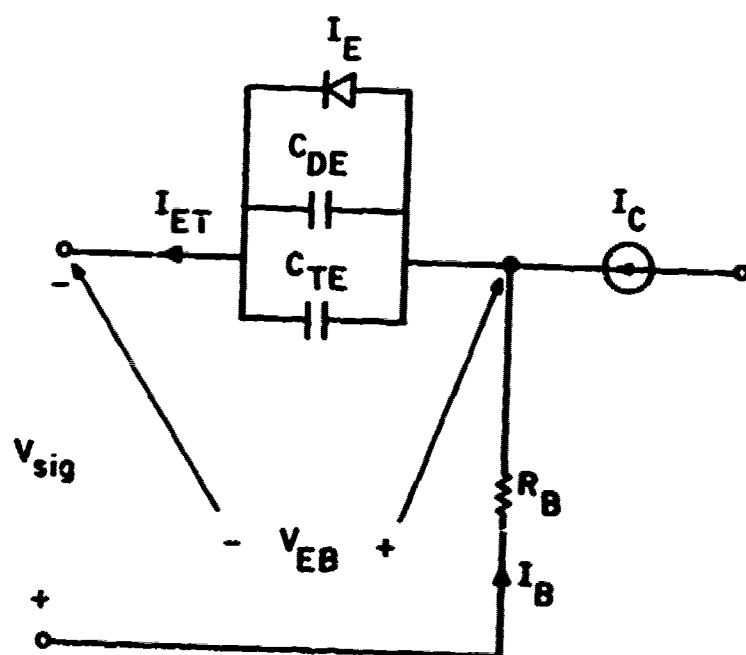
FIG. 4.3   EQUIVALENT CIRCUIT FOR THE

EMITTER-BASE REGION.

which is the differential equation to be solved numerically by the computer program EBCP. This differential equation is a first-order ordinary differential equation of the form

$$\frac{df}{dt} = g(t,f)$$

and can be solved by the fourth-order Runge-Kutta method:

$$f(t + \Delta t) = f(t) + \frac{\Delta t}{6} (k_1 + 2k_2 + 2k_3 + k_4) , \qquad (4.23)$$

where $k_1 = g[t,f(t)]$,

$$k_2 = g[t + (\Delta t/2), f(t) + k_1(\Delta t/2)],$$

$$k_3 = g[t + (\Delta t/2), f(t) + k_2(\Delta t/2)] \text{ and}$$

$$k_4 = g[t + \Delta t, f(t) + k_3 \Delta t].$$

The assumption that $I_c(t)$ is a known quantity, at this point, appears artificial because I_c is known to be dependent on the electron particle current injected into the collector region which is dependent on V_{EB}, and V_{EB} is the unknown quantity being numerically evaluated. This apparent dilemma is resolved in Section 4.2.4.

4.2.3 Collector Region Large-Signal Model and the Collector Simulation Subroutine CCP.

4.2.3a Equations to be Solved and the Simulation Technique.
The collector simulation subroutine CCP consists of two parts: a large-signal simulation subprogram LSSP and a collector circuit computer subprogram CCCP. The iteration scheme is illustrated in Fig. 4.4. When CCP is called into operation, V_{CB}, J_{nB}, V_{bias}, Z_L and C_c are known quantities where

$$V_{CB} = V_{bias} + (I_{ET} - I_c)R_B \qquad (4.24)$$
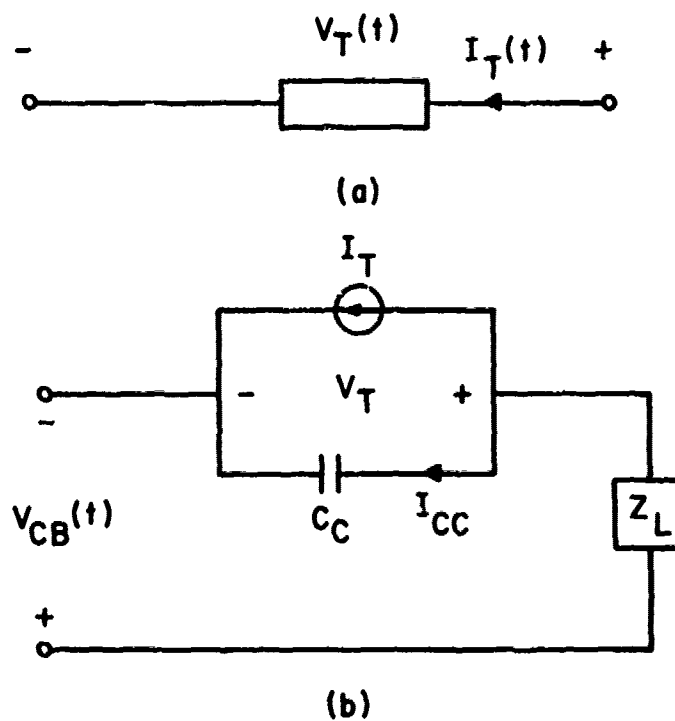
FIG. 4.4 THE COLLECTOR ITERATION SCHEME. (a) I_T IS
CALCULATED BY USING LSSP WITH V_T KNOWN AND
(b) I_{cc} AND V_T ARE CALCULATED, WITH V_{CB}, I_T,
C_c AND Z_L KNOWN, BY USING CCCP.

and

$$J_{nB} = \text{base transport factor} \times J_{nE} = \text{sech} \frac{w_B}{L_n} \times J_{nE} \quad . \quad (4.25)$$

The collector depletion capacitance[12] is given by

$$C_c = \left[C_i + \frac{R_b}{R_b + R_{bb'}} C_b \right] \text{(number of emitter-base finger pairs)} \quad ,$$
$$(4.26)$$

where

$$R_b \cong \frac{d}{2x_{B_2} \sigma_B \ell} \quad ,$$

$$R_{bb'} \cong \frac{w}{12x_{B_1} \sigma_B \ell} \quad ,$$

$$C_i = \frac{\varepsilon}{w_T} w\ell$$

and

$$C_b = \frac{2\varepsilon}{w_T} d\ell \quad .$$

The definitions of the device geometrical parameters are included in Fig. 3.2. The computer subprogram LSSP is used to calculate J_T, with V_T and J_{nB} as known quantities. The computer subprogram CCCP is used to calculate V_T, J_{cc} and J_c with V_{CB}, J_T, C_c and Z_L as given quantities. Figure 4.5 shows the block diagram of collector simulation subroutine CCP. The assumption that V_{CB} and J_{nB} are known quantities appears

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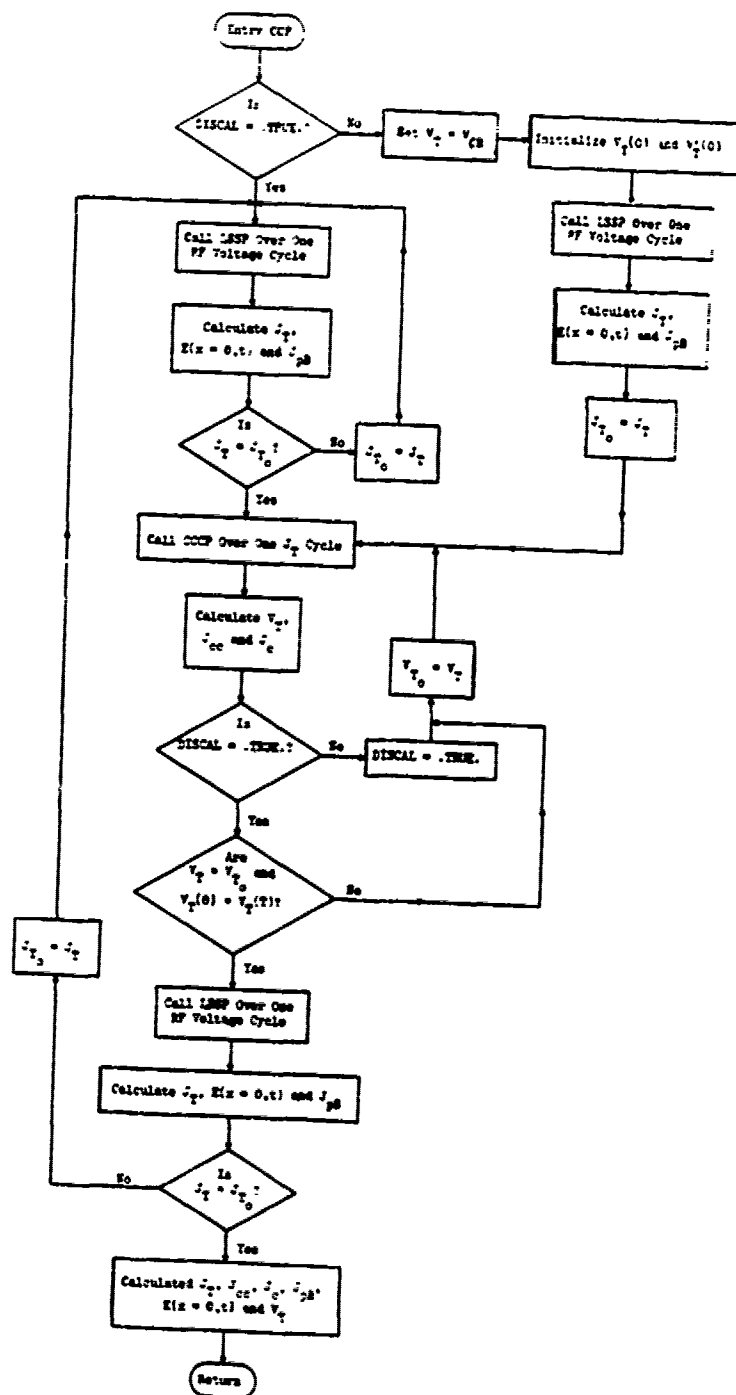
FIG. 4.5 BLOCK DIAGRAM OF LARGE-SIGNAL SUBROUTINE CCP.

artificial because V_{CB} and J_{nB} are J_c dependent and J_c is the quantity being numerically calculated. This dilemma is resolved in Section 4.2.4.

4.2.3b Subprogram LSSP. The subroutine program LSSP is based on a device simulation program developed at the Electron Physics Laboratory written from the point of view of computational efficiency by Bauhahn and Haddad.[62] The subprogram LSSP obtains a spatially one-dimensional solution of the continuity equations, Poisson's equation, and the current expressions obtained from a first-order solution of the Boltzmann transport equation. Figure 4.6 presents the basic flow of the simulation. If the electric field, carrier concentrations, V_T and J_T are known at a particular time t, Fig. 4.6 illustrates how the electric field, carrier concentrations, V_T and J_T at $t + \Delta t$ are obtained. Note that currents are defined to be positive in the direction of the electric field. The simulation is voltage driven, therefore $V_T(t + \Delta t)$ must be given. As shown in Fig. 4.6, the first step is to solve the continuity equations and obtain $p(t + \Delta t)$ and $n(t + \Delta t)$ where G is the generation rate $(C\text{-}s^{-1}\text{-}cm^{-3})$ and x is the one-dimensional spatial coordinate (cm). Carrier concentrations at $t + \Delta t$ can be obtained because the derivatives of p and n with respect to time in the finite-difference approximations include $p(t + \Delta t)$ and $n(t + \Delta t)$ terms. The second step is using Poisson's equation to obtain $E(t + \Delta t)$ to within a constant of integration. This constant is determined by requiring that the integral of the electric field across the collector region equals the base-collector voltage V_T at $t + \Delta t$. At this point, the carrier concentrations and the electric field at $t + \Delta t$ are known. In Step 3 the carrier velocities at $t + \Delta t$ are determined since the electric field at $t + \Delta t$ is known where $v_{ps,ns}$ are the saturated hole and electron

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1.

$$e \frac{\partial p}{\partial t} = G[E(x,t)] - \frac{\partial J_p(x,t)}{\partial x} \qquad (A)$$

$$\epsilon \frac{\partial n}{\partial t} = G[E(x,t)] + \frac{\partial J_n(x,t)}{\partial x} \qquad (B)$$

yields $p(t + \Delta t)$, $n(t + \Delta t)$.

2.

$$\epsilon \frac{\partial E(t + \Delta t)}{\partial x} = e[p(x,t + \Delta t) - n(x,t + \Delta t) - N_A^-(x)]$$

$$\text{subject to: } V_T(t + \Delta t) = \int_0^{W_T} E(t + \Delta t) \, dx$$

yields $E(t + \Delta t)$

3.

$$v_{p,n}(t + \Delta t,x) = v_{ps,ns}\left\{1 - \exp\left[-E(x,t + \Delta t)\mu_{p,n}/v_{ps,ns}\right]\right\}$$

yields $v_{p,n}(t + \Delta t,x)$

4.

$$J_p(x,t + \Delta t) = ep(x,t + \Delta t)v_p(x,t + \Delta t) - eD_p \frac{\partial p(t + \Delta t)}{\partial x}$$

$$J_n(x,t + \Delta t) = en(x,t + \Delta t)v_n(x,t + \Delta t) + eD_n \frac{\partial n(t + \Delta t)}{\partial x}$$

$$J_T^{(t+\Delta t)} = \frac{1}{W_T} \int_0^{W_T} [J_p(t + \Delta t) + J_n(t + \Delta t)] \, dx$$

yields $J_{p,n}(x,t + \Delta t)$

5.

$$G[E(x,t + \Delta t)] = A_p \exp\left[-b_p/E(x,t + \Delta t)\right]|J_p(x,t + \Delta t)|$$

$$+ A_n \exp\left[-b_n/E(x,t + \Delta t)\right]|J_n(x,t + \Delta t)|$$

FIG. 4.6 EQUATIONS SOLVED AND SEQUENCE OF STEPS.

velocities ($cm-s^{-1}$) and $\mu_{p,n}$ are the hole and electron low-field mobilities ($cm-V^{-1}-s^{-1}$), respectively. Step 4 shows the expressions used to calculate the current densities at $t + \Delta t$ where $J_{p,n}$ are the hole and electron current densities and J_T is the collector terminal particle current density which is found by integrating the particle current densities throughout the collector region. It should be pointed out that J_T is not the total collector current density because it does not include the displacement current, which must be supplied externally. The total current density at any point x is a constant and can be written as follows:

$$J_c = J_p(x) + J_n(x) + \epsilon \frac{\partial E}{\partial t} \quad . \tag{4.27}$$

Integrating from $x = 0$ to $x = w_T$ yields

$$J_c = \frac{1}{w_T} \int_0^{w_T} [J_p(x) + J_n(x)] \, dx + \frac{\epsilon}{w_T} \frac{\partial}{\partial t} \int_0^{w_T} E(x) \, dx$$

$$= J_T + \frac{\epsilon}{w_T} \frac{\partial V_T}{\partial t} \quad . \tag{4.28}$$

Step 5 is used to determine the generation rate G whose expression is given in Step 5 of Fig. 4.6. The values of α_n and α_p are determined experimentally and can be calculated by using Tables 2.1 and 2.2. After these five steps of calculation, everything about the collector region at $t + \Delta t$ is known. A new driving voltage value at $t + 2\Delta t$ is specified and the cycle is repeated.

4.2.3c The Difference Equations in Computer Subprogram LSSP.
The difference eq   ~s used to solve the differential equations of

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Fig. 4.6 are presented here. Figure 4.7 shows the space-time grid used for the differential equations where the index K refers to the time step, the index J refers to the carrier space step, and the index I refers to the field space step.

The continuity equations are approximated by

$$\frac{(p)_J^{K+1} - (p)_J^K}{\Delta t/e} = (G)_J^K - \frac{(J_p)_I^K - (J_p)_{I-1}^K}{\Delta x} \tag{4.29}$$

and

$$\frac{(n)_J^{K+1} - (n)_J^K}{\Delta t/e} = (G)_J^K + \frac{(J_n)_I^K - (J_n)_{I-1}^K}{\Delta x} \quad , \tag{4.30}$$

where Δt is the time step; Δx is the space step; and the generation rate, assuming that only pure avalanche generation occurs in the collector region, is given by

$$(G)_J^K = \frac{1}{2}(G)_I^K + \frac{1}{2}(G)_{I-1}^K \quad , \tag{4.31}$$

where

$$(G)_I^K = (\alpha_n)_I^K |(J_n)_I^K| + (\alpha_p)_I^K |(J_p)_I^K| \quad . \tag{4.32}$$

The time step Δt is limited in this case by the dielectric relaxation time[62] which is given by

$$\Delta t \overset{\leq}{=} \tau_R \overset{\Delta}{=} \frac{\varepsilon}{e(n\mu_n + p\mu_p)} \quad , \tag{4.33}$$

where μ_n and μ_p are the electron and hole mobilities. Poisson's equation becomes

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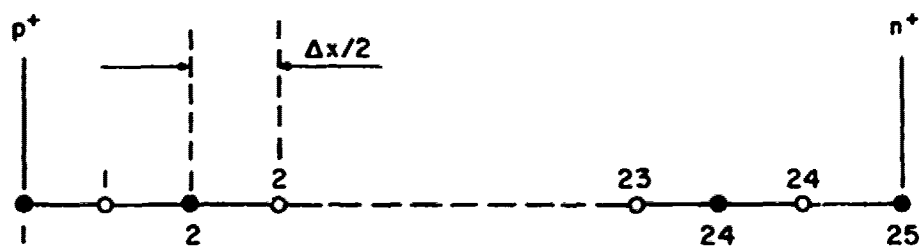
(●) CARRIER CONCENTRATIONS

(O) ELECTRIC FIELD, PARTICLE CURRENTS, GENERATION RATES

(a)
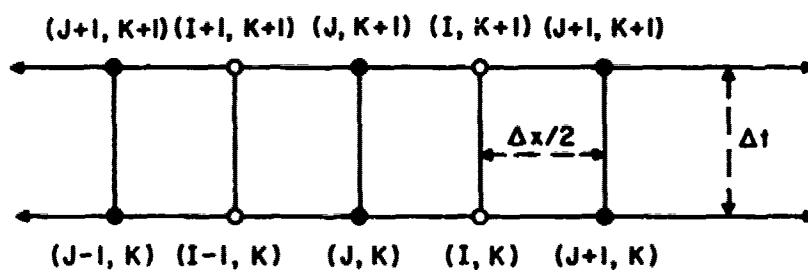
(b)

FIG. 4.7 SPACE-TIME MESH USED TO WRITE THE DIFFERENCE EQUATIONS.

(a) SPACE MESH.   (b) SPACE-TIME MESH.

$$\frac{(E)_I^K - (E)_{I-1}^K}{\Delta x} = \frac{(p)_J^K - (n)_J^K + (N_D)_J}{\varepsilon/e} \quad , \qquad (4.34)$$

where E is the electric field and N_D is the donor doping density in the collector region. The transport equations for electrons and holes become

$$(J_p)_I^K = e(p)_J^K (v_p)_I^K - e(D_p)_I^K \frac{(p)_{J+1}^{K+1} - (p)_J^{K+1}}{\Delta x} \qquad (4.35)$$

and

$$(J_n)_I^K = e(n)_{J+1}^K (v_n)_I^K + e(D_n)_I^K \frac{(n)_{J+1}^{K+1} - (n)_J^{K+1}}{\Delta x} \qquad (4.36)$$

for $(E)_I^K \gtreqless 0$ and

$$(J_p)_I^K = e(p)_{J+1}^K (v_p)_I^K - e(D_p)_I^K \frac{(p)_{J+1}^{K+1} - (p)_J^{K+1}}{\Delta x} \qquad (4.37)$$

and

$$(J_n)_I^K = e(n)_J^K (v_n)_I^K + e(D_n)_I^K \frac{(n)_{J+1}^{K+1} - (n)_J^{K+1}}{\Delta x} \qquad (4.38)$$

for $(E)_I^K \lesseqgtr 0$, where v_n and v_p are given by the expressions

$$(v_p)_I^K = v_{ps}\left[1 - \exp\left(-\frac{(E)_I^K \mu_p}{v_{ps}}\right)\right] \qquad (4.39)$$

and

$$(v_n)_I^K = v_{ns}\left[1 - \exp\left(-\frac{(E)_I^K \mu_n}{v_{ns}}\right)\right] \quad , \qquad (4.40)$$

respectively, and D_n and D_p are the field-dependent electron and hole

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diffusion coefficients. The drift terms in the current density
equations use "upwind" carriers and are explicit. The reason for
the name upwind can be seen in Eqs. 4.35 through 4.38, i.e., in
order to calculate the particle current at (I,K), the particle
concentration in the direction opposing the particle flow, in the
upwind direction, is used. The diffusion terms are implicit. This
completes the semiconductor difference equations.

The voltage constraint stated in Step 2 of Fig. 4.6,

$$V_T(t + \Delta t) = \int_0^{w_T} E(t + \Delta t) \, dx \quad , \tag{4.41}$$

can be expressed as follows:

$$(V_T)^K = \Delta x \sum_{I=1}^{NSTEP} (E)_I^K \quad , \tag{4.42}$$

where $NSTEP \triangleq w_T/\Delta x$ and the field index $I = 1,2,\ldots,NSTEP$.

The electron current density at the base-collector metallurgical
junction is assumed to be equal to the electron current density at the
edge of the base-collector depletion region since the width of the
base-collector depletion region into the base region is very small.
Most of the carrier generation occurs in the depleted collector region.
The electric field at the base-collector metallurgical junction is
always above the electric field necessary to sustain electron and hole
carrier saturation velocities. If the electron and hole carrier
densities at the base-collector metallurgical junction are defined to
be

$$n_B(t) = \frac{J_{nB}(t)}{v_{ns}}$$

and

$$p_B(t) = \frac{J_{pB}(t)}{v_{ps}},$$

respectively, where v_{ns} and v_{ps} are the electron and hole carrier saturation velocities and the avalanche multiplication produced hole current J_{pB} is calculated by the subprogram LSSP, the actual current densities at this boundary will be significantly lower than J_{nB} and J_{pB}. The reason for this is that there are large magnitude electron and hole diffusion currents flowing in the opposite direction to the drift current components. Figure 4.8 contains the schematic distribution profiles of electron and hole densities in the depleted collector region. A set of "current conserving" boundary conditions will now be derived. When the electric field is pointing in the direction opposing that of the space coordinate x, as in n-type CATT devices, the following is obtained:

$$J_p = epv_p + eD_p \frac{\partial p}{\partial x}$$

and

$$J_n = env_n - eD_n \frac{\partial n}{\partial x}$$

which can be written as

$$(J_p)_1^K = e(p)_1^K (v_p)_1^K + e(D_p)_1^K \frac{(p)_2^K - (p)_1^K}{\Delta x}$$

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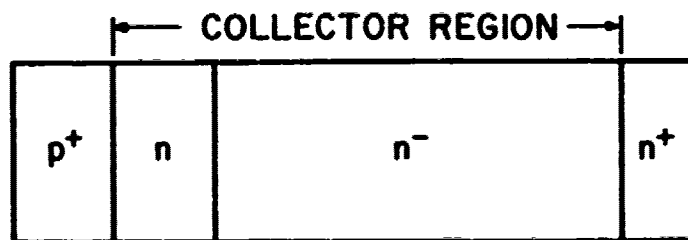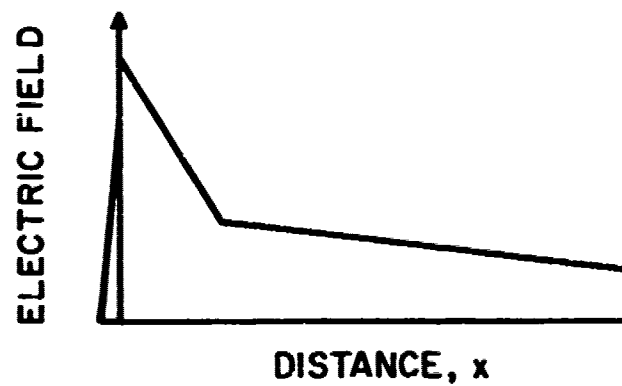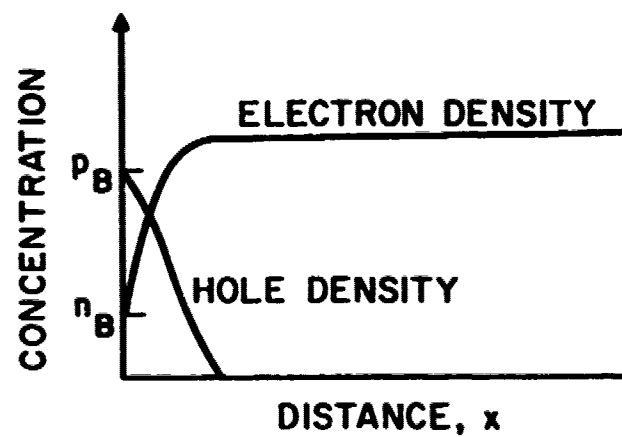
FIG. 4.8 (a) COLLECTOR REGION, (b) $|E(x)|$ PROFILE AND

(c) ELECTRON AND HOLE CONCENTRATION PROFILE.

and

$$(J_n)^K_1 = e(n)^K_1 (v_n)^K_1 - e(D_n)^K_1 \frac{(n)^K_2 - (n)^K_1}{\Delta x} \ .$$

The boundary conditions are obtained from these equations by rearranging the terms and they are

$$n_B(t) = \frac{J_{nB}(t) + eD_n(n)^K_2/\Delta x}{ev_{ns} + eD_n/\Delta x} \tag{4.43}$$

and

$$p_B(t) = \frac{J_{pB}(t) - eD_p(p)^K_2/\Delta x}{ev_{ps} - eD_p/\Delta x} \ , \tag{4.44}$$

where $n_B(t) \triangleq (n)^K_1$, $p_B(t) \triangleq (p)^K_1$, $J_{nB}(t) \triangleq (J_n)^K_1$, $J_{pB}(t) \triangleq (J_p)^K_1$ and the indexes 1 and 2 represent the space point at the metallurgical junction and the space point next to the junction, respectively. The carrier velocities are assumed to be at the saturation values and the diffusion constants have the low field values.

4.2.3d Subprogram CCCP. The circuit problem to be solved by CCCP is shown in Fig. 4.4. The differential equations to be solved are

$$\frac{dV_T}{dt} = V'_T \tag{4.45}$$

and

$$\frac{dV_T^{\bullet}}{dt} = \frac{C_L}{C_c + C_L} \frac{d^2 V_{CB}}{dt^2} + \frac{1}{C_c + C_L} \frac{1}{R_L} \frac{dV_{CB}}{dt} - \frac{1}{C_c + C_L} \frac{dI_T}{dt}$$

$$+ \frac{1}{C_c + C_L} \frac{1}{L_L} V_{CB} - \frac{1}{C_c + C_L} \frac{1}{R_L} V_T^{\bullet} - \frac{1}{C_c + C_L} \frac{1}{L_L} V_T \quad , \quad (4.46)$$

and they are of the form

$$\frac{df_1}{dt} = g_1(t,f_1,f_2)$$

and

$$\frac{df_2}{dt} = g_2(t,f_1,f_2) \quad .$$

Their solutions can be obtained by using the fourth-order Runge-Kutta method.

4.2.4 Iteration Scheme Which Couples the Emitter-Base Region and the Collector Region Simulations. Previously, the details of EBCP and CCP (LSSP and CCCP) were discussed. The iteration scheme which couples EBCP and CCP is described in Fig. 4.9 which is the block diagram of the complete large-signal computer simulation program.

4.3 Sample Results

Large-signal simulations using EBCP and CCP, determine I_E, I_{CTE}, I_{CDE}, V_{EB}, V_{EBJ}, J_{nB}, I_T, I_{pB}, I_{cc}, I_c and V_T. From these results the CATT amplifier output RF power, power gain and efficiency can be determined. Figure 4.10a shows the waveforms of J_{nB}, J_T and V_T for the case in which the load is a high-Q tank circuit whose resonant frequency is tuned to the signal frequency. Figure 4.10b

FIG. 4.9 BLOCK DIAGRAM OF THE COMPLETE LARGE-SIGNAL

SIMULATION PROGRAM.

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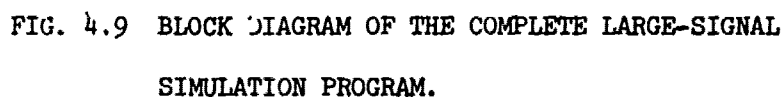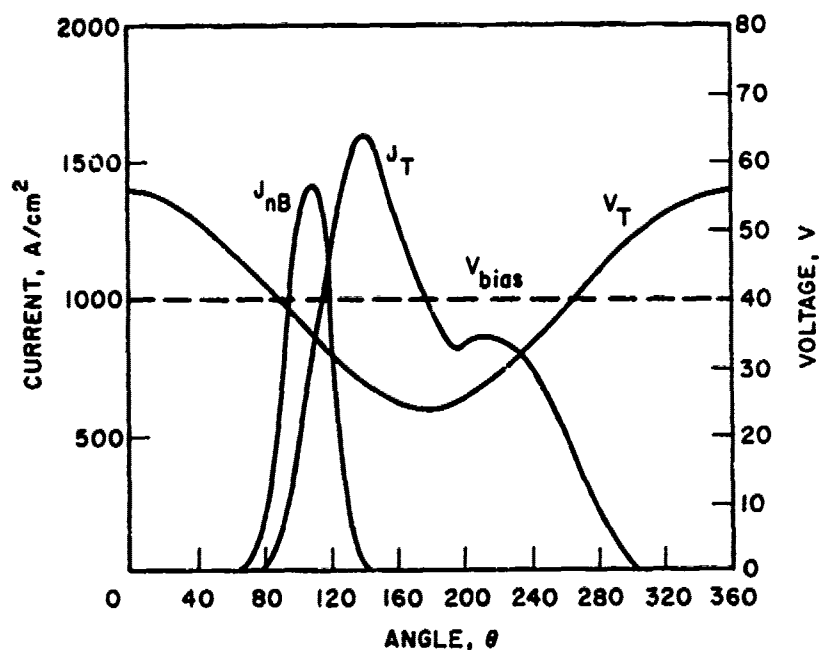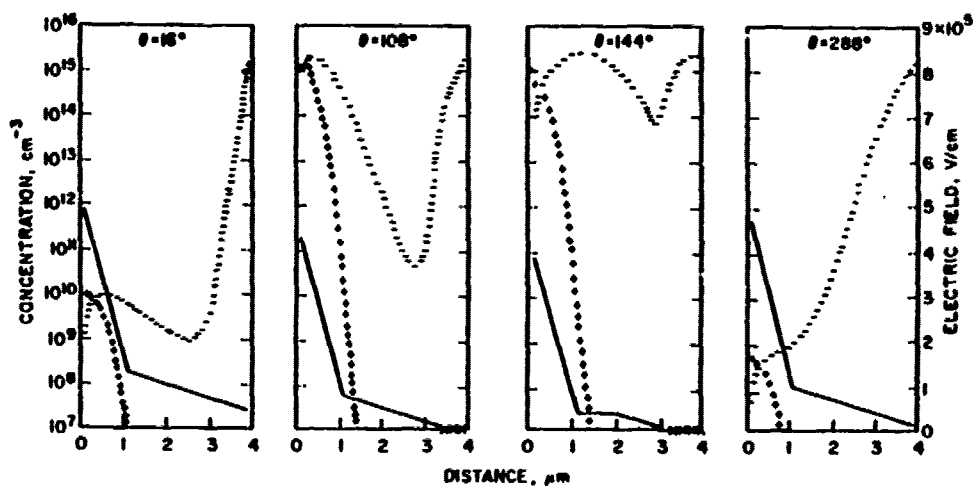
FIG. 4.10 (a) J_{nB}, J_T AND V_T WAVEFORMS AND (b) DISTRIBUTION
PLOTS OF ELECTRON DENSITY (MINUS SIGNS), HOLE DENSITY
(PLUS SIGNS), AND ELECTRIC FIELD PROFILE (SOLID LINES).
(×××× REPRESENTS THE REGION WHERE THE ELECTRIC FIELD
HAS REVERSED ITS DIRECTION)

shows the distribution plots of electron and hole densities and the
electric field profile at various phase angles. At $\theta = 18$ degrees
an insignificant number of electrons is injected into the collector
region, at $\theta = 108$ degrees a large number of electrons is injected and
they undergo avalanche multiplication, at $\theta = 144$ degrees electron
carriers drift across the depleted collector region, and at $\theta = 288$
degrees most of the electron carriers have been collected at the collector
contact.

4.4 Improvements Over Previous Large-Signal Simulation of Class C CATT Amplifiers

The computer large-signal simulation program described in this
chapter has eliminated the following inadequacies contained in the large-
signal simulation by Yu et al.:[33]

1. Emitter-base high-injection level effects were not incorporated.

2. Effects of high emitter doping level, minority carrier induced
electric field in the base region, and a nonzero minority carrier density
at the base-side edge of the base-collector depletion region were
ignored.

3. The Early effect was ignored.

4. Diffusion currents in the depleted collector region were
ignored.

5. A current nonconserving boundary condition for minority
carriers in the depleted collector region was employed.

6. In determining the feedback hole current in an n-type CATT
device, a time-averaged carrier multiplication factor was used which

is valid only if the emitter-base injected charge is very narrow and
the carriers generated due to the base-collector reverse saturation
current are negligible.

4.5 Conclusions

In this chapter, analytical expressions for the circuit model of
the emitter-base region were derived. These expressions are valid at
any injection level. The Early effect, high emitter doping density
effect, and nonzero $n(w_3)$ effect were taken into consideration. The
collector region is modeled by employing a difference-equations version
of the semiconductor differential equations. Descriptions were given
for the numerical methods used. Field dependences of charge carrier
drift velocities, diffusion constants and ionization coefficients,
and the space-charge effect were included in modeling the collector
region. The iteration scheme which couples the emitter-base circuit
model and the collector region is described. The iteration scheme
is constructed in such a way that the time step size for EBCP, LSSP and
CCCP can be independently different from each other. This feature is
very convenient and can save much unnecessary simulation cost.

CHAPTER V.   LARGE-SIGNAL STUDIES FOR CLASS C CATT AMPLIFIERS

AND COMPARISON WITH CLASS C BJT AMPLIFIERS

5.1 Introduction

In this chapter large-signal results of Class C CATT and BJT
amplifiers are obtained from the computer simulation model developed
in the previous chapter. This study is concerned with a series of
X-band CATT devices with uniformly doped and HI-LO collector structures
and a series of X-band BJTs with uniformly doped collector structures.
The main distinction between the CATT devices and the BJTs is that the
avalanche multiplication factor of the latter is always limited to
1.1 or less. The effects of impurity doping levels and widths of the
base and the collector regions and the optimum dc bias and load are
investigated at various input power levels and operating frequencies.
The Class C CATT and BJT amplifiers are compared on the basis of their
efficiency, power gain, and the device inherent bandwidth.

5.2 Large-Signal Simulation Results for Class C CATT Amplifiers

5.2.1 General Discussion. The following study shows the
effects of avalanche multiplication and wide collector regions. Large-
signal simulations of Class C CATT amplifiers with various impurity
doping levels and widths of the base and collector regions are carried
out. The usefulness and the limitation of carrier multiplication and
long collector transit angles are explored. The optimum values of the
device parameters are determined. The amplifier inherent bandwidth,
dynamic range, power gain, efficiency, optimum dc bias and optimum
load are investigated.

The following large-signal simulations used the label DEV:material, type, letter, N_c (cm^{-3}), w_T (μm) for devices with uniformly doped collectors and DEV:material, type, letter, N_{av} (cm^{-3}), w_{av} (μm), N_{drift} (cm^{-3}), w_D (μm) for devices with HI-LO collector regions, where the symbols N_c, w_T, N_{av}, w_{av}, N_{drift} and w_D have been defined previously. Therefore, DEV:Si,n,A,2 x 10^{16},1.1,1 x 10^{15},2.9 is the label used for a Si device which has an emitter-base structure A and a collector structure whose avalanche multiplication region is impurity doped at 2 x 10^{16} cm^{-3} and is 1.1 μm wide, and whose drift region is impurity doped at 1 x 10^{15} cm^{-3} and is 2.9 μm wide. The geometrical dimensions and the impurity doping levels of the emitter-base structures simulated are listed in Table 5.1.

5.2.2 Optimum Load. The optimum load for a Class C CATT amplifier is the same as that for a Class C BJT amplifier. To obtain maximum RF power at the fundamental harmonic, the load should be a high Q, parallel RLC tank circuit which, in combination with the collector cold capacitance C_c, has a resonant frequency equal to that of the emitter-base driving signal. With such a load, a typical set of $J_T(t)$, $V_T(t)$ and the emitter-base injected charge carrier waveforms is shown in Fig. 5.1 where the effective dynamic multiplication factor M_A is defined as:

$$M_A = \frac{\int_0^T J_T(t)\, dt}{\int_0^T [J_{nB}(t) + J_{c_{ns}} + J_{c_{ps}}]\, dt} \qquad (5.1)$$

and η is the overall amplifier efficiency. The aforementioned optimum load condition can be derived as follows. The average output power is

Table 5.1

Emitter-Base Structural Parameters

Emitter-Base Structure	N_D (1/cm^3)	w_{E_o} (μm)	N_A (1/cm^3)	w_{B_o} (μm)	x_{B_1} (μm)	x_{B_2} (μm)	w (μm)	d (μm)	ℓ (μm)	h (μm)	Emitter-Base Finger Pairs	A_E (cm^2)
A	1×10^{19}	0.3	5×10^{17}	0.3	0.3	0.6	0.75	1.55	30	4	10	2.25×10^{-6}
B	5×10^{19}	0.4	2.5×10^{17}	0.25	0.25	0.65	0.6	0.2	20	4	14	1.68×10^{-6}
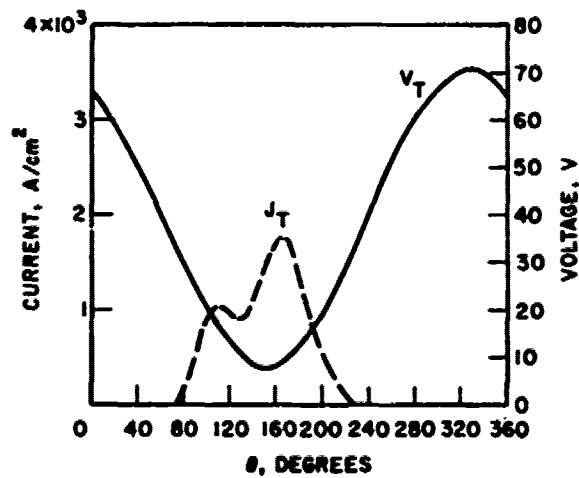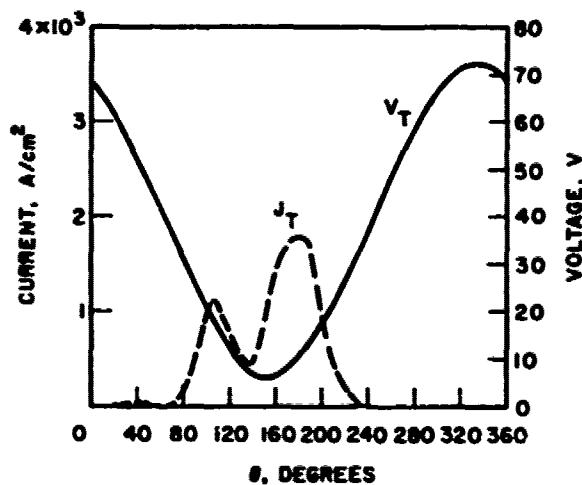
FIG. 5.1 (a) J_T AND V_T WAVEFORMS WHEN R_L IS OPTIMUM

(G_p = 9.74 dB, η = 55 PERCENT, V_{RF} = 31.3 V

AND M_A = 1.036). (b) J_T AND V_T WAVEFORMS WHEN

R_L IS GREATER THAN THE OPTIMUM VALUE (G_p =

9.15 dB, η = 52 PERCENT, V_{RF} = 33 V, M_A =

1.053). (DEV:Si,n,B,6 x 10^{15},2; f = 12.75 GHz;

$V_{sig}(t)$ = 1.1 sin ωt - 0.191 V; V_{bias} = 40 V)

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given by

$$P_{out} = \frac{1}{T} \int_0^T I_c(t) V_T(t) \, dt \quad , \tag{5.2}$$

where T is the RF period. Since $I_c(t) = I_T(t) + C_c(dV_T/dt)$,

$$P_{out} = \frac{1}{T} \int_0^T I_T(t) V_T(t) \, dt \quad . \tag{5.3}$$

If $I_T(t)$ and $V_T(t)$ are expressed in terms of their harmonic components, Eq. 5.3 becomes

$$P_{out} = I_{T_{dc}} V_{T_o} + |I_{T_1}||V_{T_1}| \cos \theta_1 + |I_{T_2}||V_{T_2}| \cos \theta_2 + \ldots + |I_{T_n}|$$
$$\cdot |V_{T_n}| \cos \theta_n + \ldots, \tag{5.4}$$

where θ_n is the phase difference between the nth harmonic components of $I_T(t)$ and $V_T(t)$. Under optimum load conditions, current component I_{T_1} sees a nearly pure resistive load and all higher harmonics of $I_T(t)$ see nearly a zero impedance. Therefore, θ_1 is approximately π rad and $V_{T_n} \simeq 0$ V for $n \overset{\geq}{=} 2$.

The resistor R_L of the parallel RLC load should be such that an optimum $V_T(t)$ is produced. For a given dc bias, if R_L is below the optimum value, a small amplitude V_T is produced which means less output power. If R_L is too large, an overly large V_T will be impressed across the collector region which will cause a decrease in both the amplifier efficiency and the available power to the load. This may be due to two different reasons or to a combination of the two depending on the dc bias. First, an extremely large-amplitude RF voltage causes the electric field in significant portions of the drift region to be depressed below

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that necessary to sustain carriers at a saturated velocity during a
significant portion of their transit across the drift region. Two
consequences follow which reduce the efficiency and the output power.
The $J_T(t)$ and $V_T(t)$ waveforms corresponding to this situation are
shown in Fig. 5.1. The slowing down of charge carriers caused the large
depression in the $J_T(t)$ waveform which is highly detrimental to the
efficiency and power output since the depression occurs near the
minimum of $V_T(t)$. The slowing down of the charge carriers also caused
an expansion in the width of the $J_T(t)$ waveform which means lower
efficiency. The reduction in efficiency is more severe at higher
collector transit angles due to the functional dependence of efficiency
on $\sin(\theta_T/2)/(\theta_T/2)$ where $\theta_T = \omega w_T/v_s$. If $\theta_T = \pi$ rad, an expansion
in the width of the $J_T(t)$ waveform could mean that large conduction
current would be flowing during the positive half-cycle of the nearly
sinusoidal $V_T(t)$ which means energy dissipation. Second, having a
large-amplitude RF voltage impressed across the collector causes the
electric field in the avalanche multiplication region to become
extremely high when $V_T(t)$ is maximum so that a significant pulse of
charge, produced by the avalanche multiplication of the thermally
generated collector reverse saturation current, is injected into the
drift region. This pulse of charge is injected much earlier than the
emitter-base injected pulse of charge. Thus, the effective width
of the $J_T(t)$ waveform is significantly increased and therfore the
efficiency is reduced drastically. The J_T and V_T waveforms corresponding
to the second case are shown in Fig. 5.2.

5.2.3 Dc Bias. It was mentioned previously that a high-efficiency,
high-gain CATT amplifier requires a dc bias such that both a

-150-
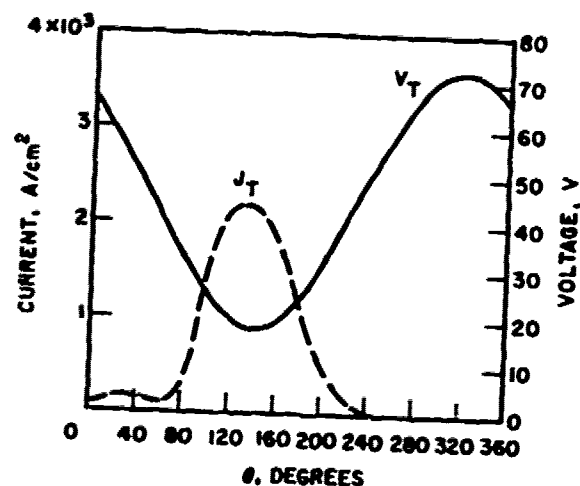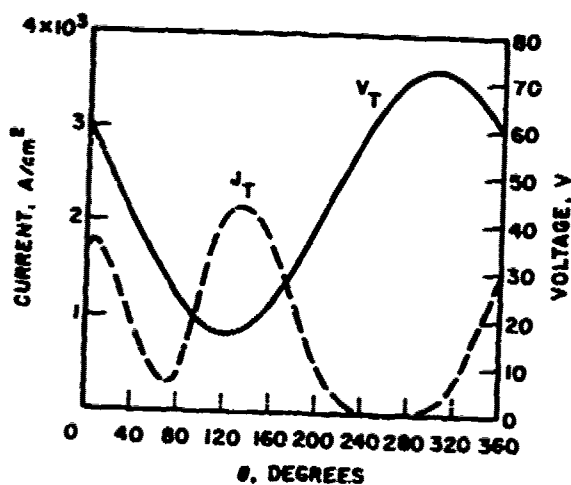
FIG. 5.2 (a) J_T AND V_T WAVEFORMS WHEN R_L IS OPTIMUM

(G_p = 10.75 dB, η = 43 PERCENT, V_{RF} = 27.2 V

AND M_A = 1.107). (b) J_T AND V_T WAVEFORMS WHEN

R_L IS GREATER THAN THE OPTIMUM VALUE (G_p = 7.37 dB,

η = 20.9 PERCENT, V_{RF} = 28 V AND M_A = 1.67).

(DEV:Si,n,B,6 x 10^{15},2; f = 12.75 GHz; $V_{sig}(t)$ =

1.1 sin ωt - 0.191 V; V_{bias} = 45 V)

large-amplitude $V_T(t)$ and a significant multiplication factor occur.
The effects of the dc bias on the amplifier performance can be illustrated
by the results given in Table 5.2. Figure 5.3 shows the optimum J_T and
V_T waveforms of a typical 4-μm CATT device at different dc biases. The
operating frequency is 12.75 GHz. The optimum dc bias is 65 V. At a
lower dc bias, i.e., 60 V, both the allowed amplitude of $V_T(t)$ and the
multiplication factor are reduced. The output power, power gain and
efficiency are also decreased. At a dc bias higher than the timum
value, i.e., 80 V, although the multiplication factor is higher, the
allowed amplitude of $V_T(t)$ decreases drastically which leads to lower
output power, lower power gain and lower efficiency. The drastic
reduction of the amplitude of V_T is due to the fact that when the dc
bias is significantly higher than the optimum value, a large-amplitude
$V_T(t)$ would cause an injection of a charge pulse at a phase angle much
earlier than the emitter-base injected signal charge. This prematurely
injected pulse of charge is the result of avalanche multiplication of
the thermally generated collector reverse saturation current under an
extremely high electric field. The effective width of $J_T(t)$ widens,
therefore, efficiency decreases. The device also loses its controlled
avalanche characteristics.

When the emitter-base driving signal is varied in its amplitude,
the amount of charge carriers injected into the collector region varies
as well. It was found that as the amplitude of the driving signal
increases the optimum dc bias for optimum gain and efficiency decreases
slightly. This is due to the space-charge effect of the injected
charge carriers from the emitter-base junction. A larger number of
injected carriers results in lower carrier multiplication, and the

Table 5.2

Effects of Dc Bias on Amplifier Performance

DEV:Si,n,A,2.2×10^{16},1.1,2×10^{15},2.9; V_{sig} = 1.15 sin ωt - 0.2 V; f = 12.75 GHz

V_{bias} (V)	RF Voltage Amplitude (V)	M_A	P_{out} (W/cm^2)	η (Percent)
57.5	12	6.25	7.5×10^3	10
55	17	5.65	8.5×10^3	16.5
52.5	24	5.5	8.5×10^3	25
50	28.5	5.5	8.5×10^3	28
42.5	22.5	4.6	5.25×10^3	22.5

DEV:Si,n,B,6×10^{15},4; V_{sig} = 1.1 sin ωt - 0.191 V; f = 12.75 GHz

V_{bias} (V)	RF Voltage Amplitude (V)	M_A	P_{out} (W/cm^2)	η (Percent)	G_p (dB)
80	12.5	2.3	2.4×10^4	10	11.77
73	30.1	1.83	2.98×10^4	25	14.13
65	42.4	1.75	2.96×10^4	38.1	15.24
60	38.7	1.71	2.63×10^4	34.1	14.58
55	31.8	1.43	2.09×10^4	32.9	13.22
35	12.9	1.09	8.197×10^3	21.4	8.05

(Cont.)

Table 5.2 (Cont.)

DEV:Si,n,B,1×10^{16},4; V_{sig} = 1.1 sin ωt - 0.191 V; f = 12.75 GHz

V_{bias} (V)	RF Voltage Amplitude (V)	M_A	P_{out} (W/cm^2)	η (Percent)	G_p (dB)
55	17.4	3.1	2.985×10^4	20.7	12.99
52.5	26.4	2.76	3.47×10^4	26.8	14.55
50	31	2.69	3.384×10^4	25.1	14.86
47.5	27.8	2.41	2.7×10^4	22.6	13.73
45	24.4	2.12	2.088×10^4	20	12.43
40	15.5	1.53	1.23×10^4	17.1	9.65
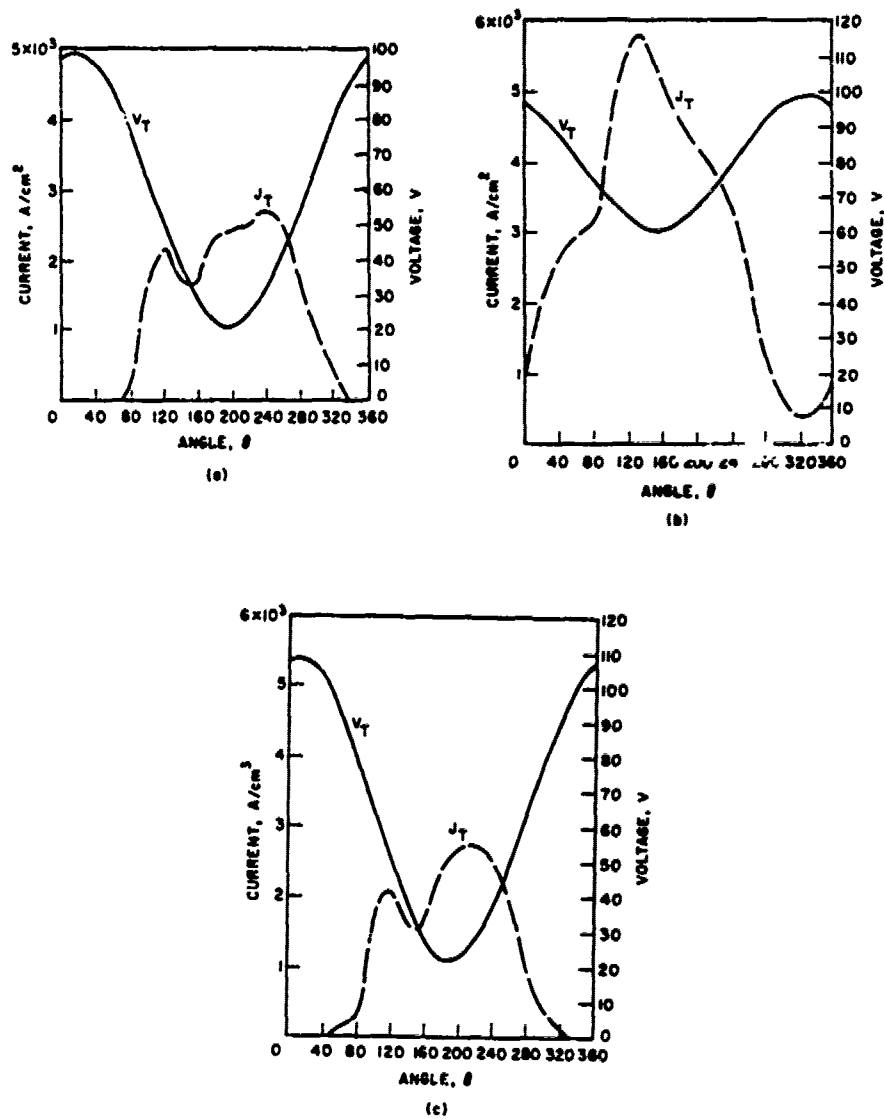
FIG. 5.3 J_T AND V_T OF A TYPICAL 4×10^{-4} cm COLLECTOR

DEVICE OPERATING AT 12.75 GHz AND MAXIMUM ALLOWED

RF VOLTAGE AMPLITUDE. (a) DC BIAS BELOW THE

OPTIMUM VALUE, (b) DC BIAS ABOVE THE OPTIMUM VALUE,

AND (c) AT OPTIMUM DC BIAS. (DEV:Si,n,B,6 x 10^{15},4)

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importance of carrier multiplication in determining the amplifier

gain and output power of a given CATT device at the optimum operating

condition relative to that of the RF voltage amplitude is reduced.

The variation in optimum dc bias as a function of the emitter-base

driving signal level is illustrated in Table 5.3. The space-charge

effect is illustrated in Figs. 5.4 and 5.5. Plots of electric field

profile, electron and hole distributions at various phase angles, and

J_T and V_T waveforms corresponding to two different emitter-base

signal levels are shown. The device is DEV:Si,n,B,6 x 10^{15},4.

The profiles of the electric field at various phase angles explain

the reduction of M_A as the driving signal level is increased. It is

also observed that V_{sus}, the minimum allowed V_T, is lower due to space

charge and therefore the maximum allowed RF voltage amplitude increases

slightly with increasing V_{sig}, assuming V_{bias} is kept constant.

The optimum dc bias also varies with the operating frequency.

It was found that, for a given device, the optimum dc bias increases

with increasing operating frequency. This is because as the operating

frequency increases the transit angle increases; therefore, charge

carriers are injected into the depleted collector earlier in a given

cycle when the value of $V_T(t)$ is higher. Avalanche multiplication

becomes a more important factor in determining the gain and the RF

output power. Avalanche multiplication is a sensitive function of the

electric field. The variation of optimum dc bias with operating

frequency is illustrated by the results tabulated in Table 5.4.

5.2.4 Effects of N_{av}, w_{av}, N_{drift} and w_D in HI-LO Collector

Structures. The effects of varying N_{av}, w_{av}, N_{drift} and w_D are

examined in this section. The results given in Table 5.5 give the

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Table 5.3

Variation of Optimum Dc Bias with Emitter-Base Signal Level

DEV:Si,n,B,1 x 10^{16},4; f = 12.75 GHz

V_{sig} (V)	Optimum Dc Bias (V)	RF Voltage Amplitude (V)	M_A
1.05 sin ωt − 0.1823	55	26.3	3.98
1.10 sin ωt − 0.191	51.5	29	2.71
1.15 sin ωt − 0.199	51	31	1.75
1.20 sin ωt − 0.2083	48.5	34	1.57
1.25 sin ωt − 0.217	46	38.1	1.45

DEV:Si,n,B,6 x 10^{15},4; f = 12.75 GHz

V_{sig} (V)	Optimum Dc Bias (V)	RF Voltage Amplitude (V)	M_A
1.05 sin ωt − 0.1823	70	40	2.55
1.10 sin ωt − 0.191	65	42.4	1.75
1.15 sin ωt − 0.199	64	49.6	1.57
1.2 sin ωt − 0.2084	63.5	50	1.37
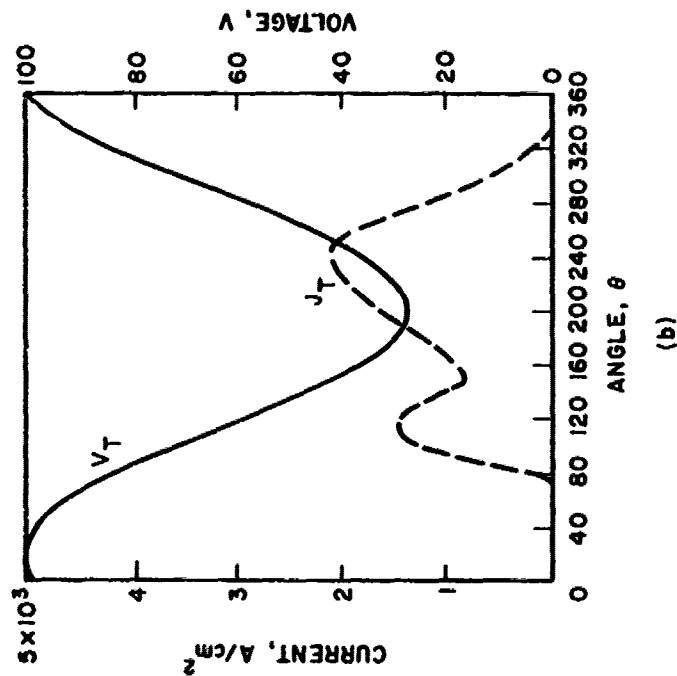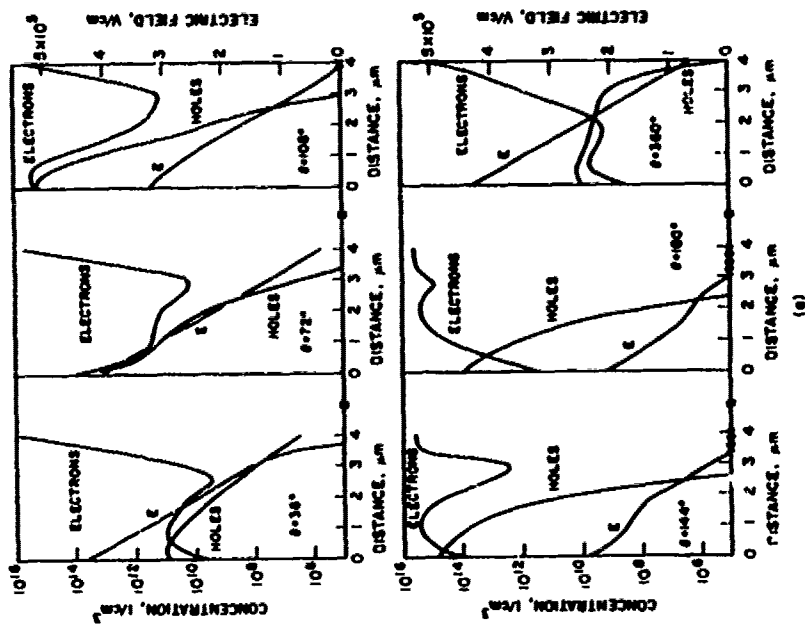
FIG. 5.4 (a) ELECTRIC FIELD PROFILE AND ELECTRON AND HOLE DISTRIBUTIONS AT VARIOUS PHASE

ANGLES. (b) J_T AND V_T WAVEFORMS. (DEV:Si,n,B,6 x 10^{15},4; f = 12.75 GHz; V_{bias} =

65 V; V_{sig} = 1.05 sin ωt - 0.1823 V; and ×××× REPRESENTS THE COLLECTOR REGION WHERE

THE ELECTRIC FIELD IS NEGATIVE)

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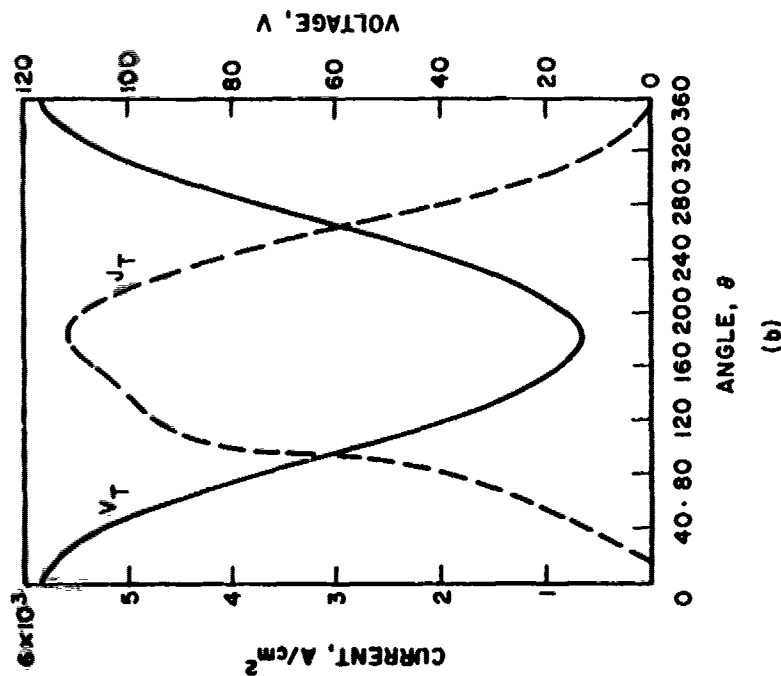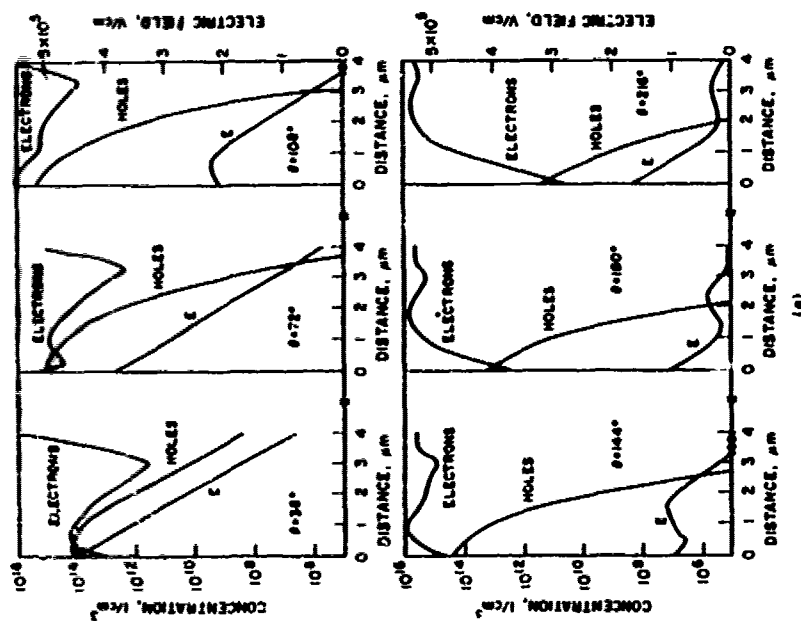
FIG. 5.5 (a) ELECTRIC FIELD PROFILE AND ELECTRON AND HOLE DISTRIBUTIONS AT VARIOUS PHASE ANGLES. (b) J_T AND V_T WAVEFORMS. (DEV:Si,n,B,6 x 10^{15},4; f = 12.75 GHz; V_{bias} = 65 V; V_{sig} = 1.2 sin ωt - 0.2083 V; AND xxx REPRESENTS THE COLLECTOR REGION WHERE THE ELECTRIC FIELD IS NEGATIVE)

Table 5.4

Variation of Optimum Dc Bias with Operating Frequency

$$(DEV:Si,n,B,2.2 \times 10^{16},1.1,2 \times 10^{15},2.9)$$

$V_{sig} = 1.1 \sin \omega t - 0.191$ V

f (GHz)	Optimum Dc Bias (V)
7	50
10	52.5
12.75	52.5
14	55
18	57
21	57.5

$V_{sig} = 1.05 \sin \omega t - 0.1823$ V

7	50
12.75	52.5
21	57.5

$V_{sig} = 1.0 \sin \omega t - 0.1736$ V

7	50
12.75	52.5
21	55

Table 5.5

Effects of N_{av} on the Performance of Class C CATT Amplifiers

DEV:Si,n,A,N_{av},1.1,2x10^{15},2.9; $V_{sig}(t) = 1.15 \sin \omega t - 0.2$ V;
f = 12.75 GHz

N_{av} (1/cm^3)	Optimum Dc Bias (V)	M_A	RF Voltage Amplitude (V)	η (Percent)	G_p (dB)
1.6x10^{16}	67.5	4.1	41	33	2.69
1.8x10^{16}	62.5	4.4	36	32	3.83
2x10^{16}	57.5	5.5	33.5	30.5	4.1
2.2x10^{16}	50	5.5	27.5	28	4.62
2.4x10^{16}	45	5.7	21	24	4.16
2.6x10^{16}	40	6.35	15.7	18.5	3.33

DEV:Si,n,B,N_{av},0.6,2x10^{15},3.4; $V_{sig}(t) = 1.1 \sin \omega t - 0.191$ V;
f = 12.75 GHz

N_{av} (1/cm^3)	Optimum Dc Bias (V)	M_A	RF Voltage Amplitude (V)	η (Percent)	G_p (dB)
1x10^{16}	75	1.2	43	32	13.2
2.5x10^{16}	67.5	1.5	50	41	15.1
3x10^{16}	66.5	1.82	52.7	39.5	15.6
4x10^{16}	57.5	2.2	40.5	30	15.2

(Cont.)

Table 5.5 (Cont.)

DEV:Si,n,B,N_{av},0.8,$2x10^{15}$,3.2; $V_{sig}(t) = 1.1 \sin \omega t - 0.191$ V;
f = 12.75 GHz

N_{av} ($1/cm^3$)	Optimum Dc Bias (V)	M_A	RF Voltage Amplitude (V)	η (Percent)	G_p (dB)
$1x10^{16}$	75	1.3	45.5	33	13.9
$1.75x10^{16}$	70	1.6	50	38.5	15.2
$2x10^{16}$	65	1.7	46.5	39	15.1
$2.25x10^{16}$	63.5	1.8	44.2	38	15.4
$2.5x10^{16}$	62	2	42	34.5	15.4
$3.5x10^{16}$	47.5	2.42	25	27.5	12.7

DEV:Si,n,B,N_{av},1.2,$2x10^{15}$,2.8; $V_{sig}(t) = 1.1 \sin \omega t - 0.191$ V;
f = 12.75 GHz

$5x10^{15}$	80	1.35	46.5	31.5	13.8
$1x10^{16}$	72.5	1.5	49.2	37.5	14.8
$1.5x10^{16}$	63.5	1.95	41	34.5	15.3
$1.75x10^{16}$	60	2.15	35	28.5	15
$2x10^{16}$	53.5	2.4	30.5	26	13.8

optimum performances of CATT devices with different N_{av} and w_{av}. For a fixed w_{av} there is a corresponding optimum N_{av}. For devices with N_{av} higher than the optimum value, larger avalanche multiplication is achieved at the device optimum dc bias, but the amplitude of V_T is decreased. The resultant efficiency, output power and power gain are lowered. If N_{av} is lower than the optimum value, although the amplitude of V_T may be slightly higher, the avalanche multiplication is lower. For devices with wider avalanche multiplication regions, the optimum N_{av} would be lower in order to maintain the device capability for large amplitude V_T. As long as the avalanche multiplication region is not too narrow or too wide, i.e., 0.6 to 1.2 µm, there is no significant difference in the performance of devices with optimized N_{av}.

The effects of drift region width and its doping level have also been examined. Large-signal simulations have been carried out for devices with emitter-base structure A. The operating frequency is kept at 12.75 GHz. The results are summarized in Table 5.6. The results indicate that the longer devices have higher optimum dc biases, higher multiplication and lower efficiencies. Higher multiplication is due to a longer collector transit angle which implies an earlier injection of carriers in a given cycle when the value of $V_T(t)$ is higher. Lower efficiency is due to its dependence on $\sin(\theta_T/2)/(\theta_T/2)$. The amplitude of V_T, output power and power gain increase with increasing w_D until w_T is approximately 5.5 µm. At $f = 12.75$ GHz, the w_T which corresponds to a π-rad collector transit angle is 4 µm. It was indicated previously that a collector transit angle greater than π rad implies a large current flow during portions of the positive half-cycle of $V_T(t)$ and, therefore, a large amount of energy dissipated. However, due to larger carrier

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Table 5.6

Effects of Drift Region Width

DEV:Si,n,A,2.2×10^{16},1.1,2×10^{15},w_D; $V_{sig}(t) = 1.15 \sin \omega t - 0.2$; $f = 12.75$ GHz

w_D (μm)	Optimum Dc Bias (V)	η (Percent)	M_A	RF Voltage Amplitude (V)	G_p (dB)
2.1	45	30	3.7	22.5	2.36
2.4	47.5	29.5	4.3	24.6	3.03
2.7	50	28	5.2	26	3.55
2.9	52.5	27.5	5.9	27	4.36
3.15	52.5	27	6.4	29	5.2
3.4	55	26.5	7.3	30.5	6.44
3.65	57.5	24.5	8.5	32.5	7.52
3.9	60	21.5	9.6	33	8.61
4.4	65	15	11.3	33.2	9.04
4.65	67.5	13.5	11	30	7.81
5.15	70	8.25	10	29	6.03

multiplication and RF voltage amplitude, the optimum w_T for maximum output power and power gain is 5.5 µm. As w_T is increased beyond 5.5 µm, efficiency becomes very low and the maximum allowed RF voltage amplitude starts to decrease. The decrease in RF voltage amplitude is due to the increase in V_{sus} with increasing w_T while the breakdown electric field intensity stays constant. If efficiency and power gain are both considered, the optimum w_T at 12.75 GHz is ~ 4.5 to ~ 4.75 µm.

The drift region doping density should be as low as possible to minimize V_{sus}, i.e., maximize the allowed RF voltage. But it should be sufficient to sustain the charge carrier density. Otherwise, the space-charge effect will force the electric field behind the charge pulse in the drift region to be depressed below the charge carrier saturation drift velocity sustaining value. As a consequence, charge carriers at the tail end of the pulse will be slowed down and the charge pulse will spread out which, in turn, will cause a decrease in the fundamental harmonic component of I_T. This is one aspect of the deterioration in amplifier power gain and efficiency due to space charge in a lightly doped drift region. Depression of electric field behind the charge pulse, when severe enough, will bring a reduction in the allowed maximum RF voltage amplitude. It can be seen from large-signal simulation results that at a low input signal level the device with the smallest N_{drift} has the largest allowed RF voltage amplitude. As the input signal level increases the allowed maximum RF voltage amplitude of the device with the smallest N_{drift} decreases noticeably. This is the other aspect of the deterioration in amplifier power gain,

power output and efficiency due to space charge in the lightly doped drift region.

Table 5.7 summarizes the results of large-signal simulations of devices with various values of N_{drift}. The electric field depression, charge pulse spreading and reduction in V_{RF} due to space charge are illustrated in Figs. 5.6 through 5.9. It is also observed that space charge in a lightly doped drift region may force up the electric field intensity near the collector contact and a significant number of electron-hole pairs will be created. This will further expand the duration of the induced current, increase power dissipation and reduce the efficiency.

5.2.5 Uniformly Doped Collector Structures. Large-signal simulations of devices with uniformly doped collectors have been carried out. The results are summarized in Table 5.8. These results correspond to the operating condition when both the power gain and the efficiency are optimized. The following observations can be made:

1. Shorter devices have higher efficiencies. The higher efficiency is due to a higher V_{RF}/V_{bias} ratio and a smaller collector transit angle. At f = 12.75 GHz, however, efficiency reaches a saturation value when the collector region width is reduced to 2 μm and it will not increase significantly if w_T is further reduced.

2. Longer devices have higher output power and power gain. The higher output power is due to a larger allowed RF voltage amplitude and a higher avalanche multiplication factor. The higher multiplication factor is due to a higher optimum dc bias and an earlier injection of charge carriers into the collector region relative to the V_T waveform.

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Table 5.7

Effects of N_{drift}

DEV:Si,n,B,2.2x10^{16},1.1,4x10^{15},2.9; f = 12.75 GHz; V_{bias} = 45 V

V_{sig} (V)	M_A	RF Voltage Amplitude (V)	η (Percent)	G_p (dB)
sin ωt − 0.1736	6.45	23.3	23.5	15.7
1.05 sin ωt − 0.1823	3.5	24.3	27.5	14.9
1.1 sin ωt − 0.191	2.35	24.7	26	13.7
1.15 sin ωt − 0.2	1.98	24.3	20.2	12.4
1.2 sin ωt − 0.2084	1.68	22	16	10.5

DEV:Si,n,B,2.2x10^{16},1.1,3x10^{15},2.9; f = 12.75 GHz; V_{bias} = 47.5 V

sin ωt − 0.1736	5.5	25	26	15.5
1.05 sin ωt − 0.1823	3.4	27.5	27	14.9
1.1 sin ωt − 0.191	2.45	28	24.5	13.9
1.15 sin ωt − 0.2	1.96	27	18.38	12.2
1.2 sin ωt − 0.2084	1.78	27.5	13.7	10.5

(Cont.)

Table 5.7 (Cont.)

DEV:Si,n,B,2.2x10^{16},1.1,2x10^{15},2.9; f = 12.75 GHz; V_{bias} = 52.5 V

V_{sig} (V)	M_A	RF Voltage Amplitude (V)	n (Percent)	G_p (dB)
0.9 sin ωt − 0.165	6.7	22.5	23.5	12.7
sin ωt − 0.1736	4.4	26.5	28	14.65
1.05 sin ωt − 0.1823	3	29.5	28	14.88
1.1 sin ωt − 0.191	2.4	30.2	23.4	14
1.15 sin ωt − 0.2	1.96	29.7	17	12.3
1.2 sin ωt − 0.2084	1.71	27.1	13.3	10.4

DEV:Si,n,B,2.2x10^{16},1.1,7.5x10^{14},2.9; f = 12.75 GHz; V_{bias} = 58.5 V

V_{sig} (V)	M_A	RF Voltage Amplitude (V)	n (Percent)	G_p (dB)
sin ωt − 0.1736	4.37	33.8	30	14.96
1.05 sin ωt − 0.1823	3.02	32	27.5	15.06
1.1 sin ωt − 0.191	2.35	31.35	19.7	13.72
1.15 sin ωt − 0.2	1.79	24.5	14.6	11.2
1.2 sin ωt − 0.2084	1.67	25.3	10.6	9.64
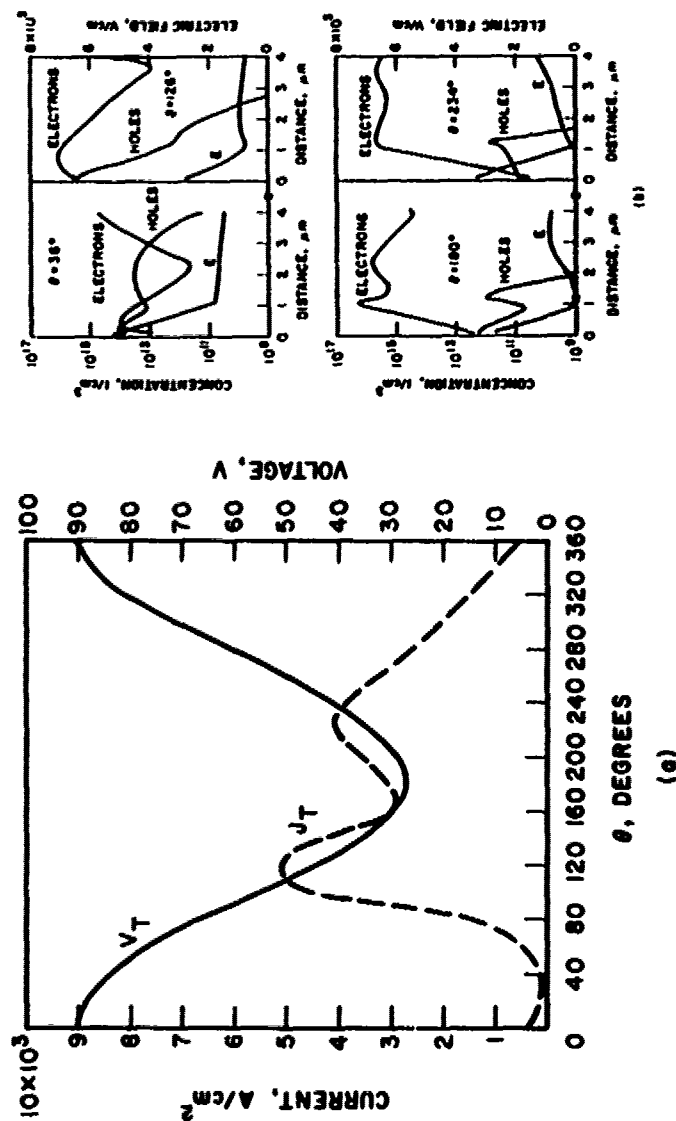
FIG. 5.6 (a) J_T AND V_T WAVEFORMS AND (b) ELECTRIC FIELD PROFILE AND ELECTRON AND HOLE DISTRIBUTIONS AT VARIOUS PHASE ANGLES. (DEV:Si,n,B,2.2 x 10^{16}, 1.1,7.5 x 10^{14},2.9; f = 12.75 GHz; V_{sig} = 1.1 sin ωt - 0.191 V; AND xxx REPRESENTS THE REGION WHERE THE ELECTRIC FIELD IS NEGATIVE)

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FIG. 5.7 (a) J_T AND V_T WAVEFORMS AND (b). ELECTRIC FIELD PROFILE AND ELECTRON AND HOLE

DISTRIBUTIONS AT VARIOUS PHASE ANGLES. (DEV:S1,n,B,2.2 x 10^{16},1.1,7.5 x 10^{14},2.9;

$f = 12.75$ GHz; $V_{sig} = 1.2$ sin $\omega t - 0.208377$ V; AND ×x× REPRESENTS THE REGION WHERE

THE ELECTRIC FIELD IS NEGATIVE)

FIG. 5.8 (a) J_T AND V_T WAVEFORMS AND (b) ELECTRIC FIELD PROFILE AND ELECTRON AND HOLE

DISTRIBUTIONS AT VARIOUS PHASE ANGLES. (DEV:S1,n,B,2.2 x 10^{16},1.1,4 x 10^{15},2.9;

$f = 12.75$ GHz; $V_{sig} = 1.1 \sin \omega t - 0.191$ V; AND xxx REPRESENTS THE REGION WHERE

THE ELECTRIC FIELD IS NEGATIVE)
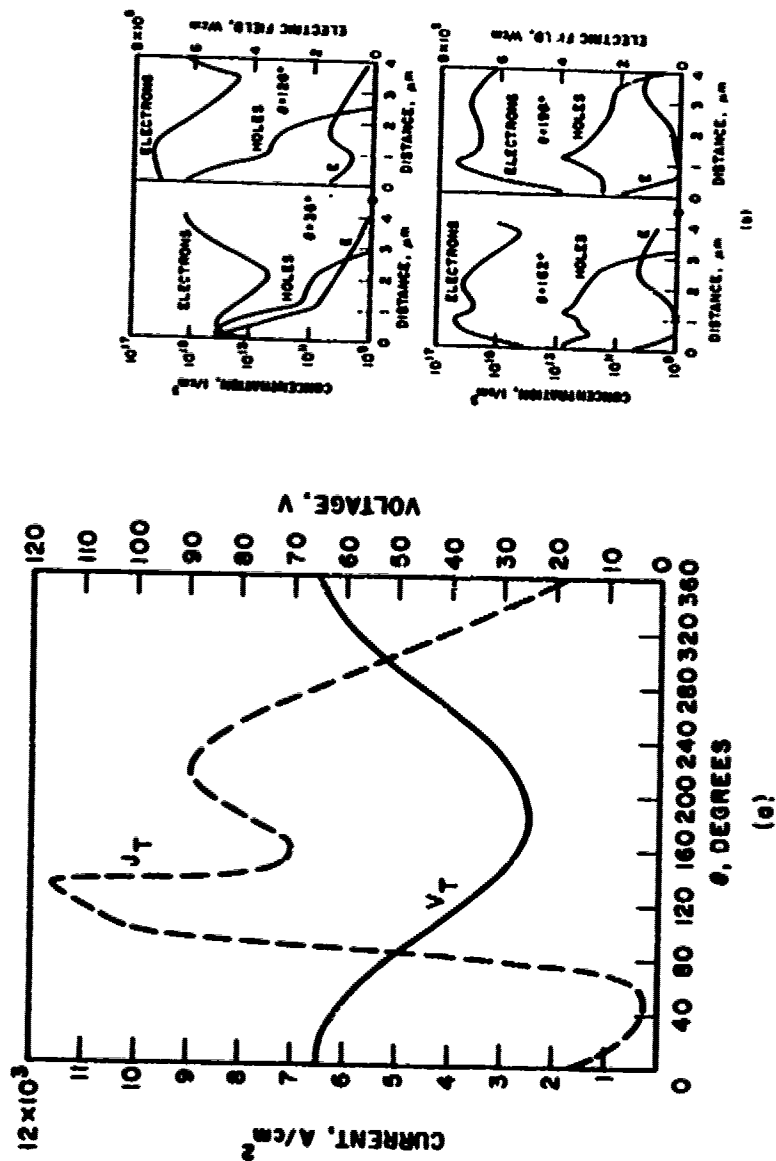
FIG. 5.9 (a) J_T AND V_T WAVEFORMS AND (b) ELECTRIC FIELD PROFILE AND ELECTRON AND HOLE DISTRIBUTIONS
AT VARIOUS PHASE ANGLES. (DEV:S1,n,B,2.2 x 10^{16},1.1,4 x 10^{15},2.9; f = 12.75 GHz; V_{sig} =
1.2 sin ωt - 0.208377 V; AND ××× REPRESENTS THE REGION WHERE THE ELECTRIC FIELD IS NEGATIVE)

Table 5.8

Large-Signal Simulation Results of CATT Devices with

Uniformly Doped Collector Structures

DEV:Si,n,B,N_c,5; f = 12.75 GHz; $V_{sig}(t) = 1.1 \sin \omega t - 0.191$ V

N_c (1/cm^3)	Optimum Dc Bias (V)	M_A	RF Voltage Amplitude (V)	η (Percent)	G_p (dB)
2x10^{15}	80	1.12	38	22	11.8
6x10^{15}	73.5	3.63	57.7	29.9	18.61
1x10^{16}	51.5	2.6	27.5	23.2	14.55
1.25x10^{16}	45	2.69	24.9	19	13.3

DEV:Si,n,B,N_c,4; f = 12.75 GHz; $V_{sig}(t) = 1.1 \sin \omega t - 0.191$ V

2x10^{15}	70	1.05	41.5	38	12.8
4x10^{15}	70	1.42	45.5	38	13.9
6x10^{15}	63.5	1.72	41.5	38.5	15.8
8.5x10^{15}	56.5	2.55	36.5	29.5	16.7
1x10^{16}	51.5	2.6	29.5	26.5	14.86

DEV:Si,n,B,N_c,3; f = 12.75 GHz; $V_{sig}(t) = 1.1 \sin \omega t - 0.191$ V

2x10^{15}	45	1.05	36.5	56.5	11.6
6x10^{15}	56.5	1.35	36	44	12.3
1x10^{16}	47.5	2.11	33	32	11.5

(Cont.)

Table 5.8 (Cont.)

DEV:Si,n,B,N_c2; f = 12.75 GHz; $V_{sig}(t)$ = 1.1 sin ωt - 0.191 V

N_C (1/cm^3)	Optimum Dc Bias (V)	M_A	RF Voltage Amplitude (V)	η (Percent)	G_p (dB)
2×10^{15}	33	1.0	28.5	55	10
6×10^{15}	37.5	1.02	29	52	10.2
1×10^{16}	40	1.06	24.4	47	10.2

3. The optimum N_c is approximately 6×10^{15} cm^{-3}. With a higher N_c, the avalanche multiplication factor may be higher at the optimum dc bias, but the permissible V_{RF} is consistently lower. The difference in the allowed V_{RF} is pronounced when $w_T \overset{\geq}{=} 3.5$ μm and $f = 12.75$ GHz. To maintain a large permissible V_{RF}, due to an increase in V_{sus} with increasing w_T, the optimum dc bias of devices with $N_c \overset{\geq}{=} 1 \times 10^{16}$ cm^{-3} actually decreases with increasing w_T if $w_T > 4$ μm. The consequences can be a decreased M_A and a decreased permissible V_{RF}. Devices with $N_c < 6 \times 10^{15}$ cm^{-3} at their optimum dc bias suffer from a smaller avalanche multiplication factor and space charge is more likely to reduce the permissible V_{RF}. The space-charge effects were discussed in Sections 5.2.3 and 5.2.4.

4. Performance of device DEV:Si,n,B,6×10^{15},4 compares very favorably with that of devices with various 4 μm HI-LO collector structures at $f = 12.75$ GHz and $V_{sig}(t) = 1.1 \sin \omega t - 0.191$ V. The results are summarized in Tables 5.5 and 5.6. A CATT device with a uniformly doped collector can be fabricated more easily. The dynamic range and inherent bandwidths of devices with HI-LO and uniformly doped collectors are compared and discussed in a later section.

5. It has been shown that V_{RF} should be as large as possible to maximize the power gain and efficiency. When V_{RF} equals the maximum permissible value, there is a considerable amount of charge carriers generated from avalanche multiplication of the charge carriers of the collector reverse saturation current during the time period when V_T is near its maximum value. This is also true for devices with HI-LO collector structures. Therefore, a more exact definition of M_A is

$$M_A = \frac{\int_0^T J_T(t) \, dt}{\int_0^T [J_{nB}(t) + J_{c_{ns}} + J_{c_{ps}}] \, dt} \quad .$$

This expression implies that the induced collector terminal current $J_T(t)$ is due to avalanche multiplication of both the charge carriers of the emitter-base injected current and the collector reverse saturation current, although the former is usually the dominant one.

5.3 Large-Signal Simulation Results for Class C BJT Amplifiers

The operation of Class C BJT amplifiers can be considered as a special mode of operation of the previously simulated three-terminal devices operated as Class C CATT amplifiers. The difference lies in the combination of collector transit angle, base-collector dc bias and amplitude of V_{RF} which results in a collector multiplication factor of 1.1 or less for BJT amplifiers.

Since avalanche multiplication does not play an important role in determining the performance of Class C BJT amplifiers, only devices with uniformly doped collectors have been simulated. The results of large-signal simulations of various Class C BJT amplifiers operating at 12.75 GHz are summarized in Table 5.9. The following observations can be made:

1. For devices with any w_T, those with the lowest N_c consistently have the best performance as long as space-charge density in the collector region is not excessively high. This is due to the restriction on M_A which makes V_{RF} the only major factor in determining amplifier performance. Higher N_c implies higher V_{sus} and V_{PT}. Higher V_{sus} and V_{PT} implies higher electric field in the vicinity of the base-collector

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Table 5.9

Large-Signal Simulation Results of Class C BJT Amplifiers

DEV:Si,n,B,N_c,5; f = 12.75 GHz; $V_{sig}(t)$ = 1.1 sin ωt − 0.191 V

N_c (1/cm³)	Optimum Dc Bias (V)	M_A	RF Voltage Amplitude (V)	η (Percent)	G_p (dB)
2x10¹⁵	70	1.06	32.9	20	10.89
6x10¹⁵	36.5	1.1	13	14.5	7.3
1x10¹⁶	always operates as a CATT amplifier when $V_{bias} \stackrel{\geq}{=} V_{PT}$				

DEV:Si,n,B,N_c,4; f = 12.75 GHz; $V_{sig}(t)$ = 1.1 sin ωt − 0.191 V

N_c (1/cm³)	Optimum Dc Bias (V)	M_A	RF Voltage Amplitude (V)	η (Percent)	G_p (dB)
2x10¹⁵	70	1.05	41.5	39	12.8
4x10¹⁵	55	1.1	21	40.5	12.55
6x10¹⁵	35	1.1	12.8	21.7	8.06
8.5x10¹⁵	32.5	1.1	10.5	13.5	6.53
1x10¹⁶	always operates as a CATT amplifier when $V_{bias} \stackrel{\geq}{=} V_{PT}$				

DEV:Si,n,B,N_c,3; f = 12.75 GHz; $V_{sig}(t)$ = 1.1 sin ωt − 0.191 V

N_c (1/cm³)	Optimum Dc Bias (V)	M_A	RF Voltage Amplitude (V)	η (Percent)	G_p (dB)
2x10¹⁵	45	1.05	36.5	56.5	11.6
6x10¹⁵	50	1.1	33.5	47	12
1x10¹⁶	27.5	1.1	14.4	20	7.5

(Cont.)

Table 5.9 (Cont.)

DEV:Si,n,B,N_c,2; f = 12.75 GHz; $V_{sig}(t)$ = 1.1 sin ωt – 0.191 V

N_c (1/cm^3)	Optimum Dc Bias (V)	M_A	RF Voltage Amplitude (V)	η (Percent)	G_p (dB)
2×10^{15}	33	1.0	28.5	55	10
6×10^{15}	37.5	1.02	29	52	10.2
1×10^{16}	40	1.06	24.4	47	10.2

junction. When M_A is restricted to 1.1 or less, therefore, devices with higher N_c have a lower maximum allowed V_{RF}. This points out one major difference in the design of CATT and BJT amplifiers.

2. Maximum power gain is achieved by the device DEV:Si,n,B,2 x 10^{15},4 while for CATT devices maximum power gain is achieved by devices with collectors 5 μm or longer. As for BJT amplifiers, longer devices have a large collector transit angle which implies that charge carriers injected from the emitter-base junction reach the multiplication region when V_T is higher. Since M_A is restricted to 1.1 or less, therefore, a longer device has a smaller maximum permissible V_{RF} when $w_T \gtrsim 3$ μm. If the collector is intrinsic or extremely lightly doped, maximum power gain would be achieved by a longer device, but the maximum current density would be limited by the aforementioned space-charge effects and therefore the device output power will be limited. The reductions in maximum permissible V_{RF} and power gain with increasing w_T are very pronounced in devices with $N_c \gtrsim 6$ x 10^{15} cm^{-3} and $w_T \gtrsim 3.5$ μm. This points out another difference in the design of CATT and BJT amplifiers.

3. Devices with $w_T \lesssim 2.5$ μm, when operating at optimum conditions, are BJT amplifiers independent of the values of N_c. The performance of the device with $N_c = 1$ x 10^{16} cm^{-3} is almost the same as that of the device with $N_c = 2$ x 10^{15} cm^{-3} at $V_{sig}(t) = 1.1 \sin \omega t - 0.191$ V. At $w_T \lesssim 2$ μm, a higher N_c may be desirable due to increased current capability of the device.

4. A shorter device has a higher efficiency.

Comparisons between the Class C CATT and BJT amplifiers are carried out in the next section.

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5.4 Comparison Between the Class C CATT Amplifier and the Class C BJT Amplifier

5.4.1 RF Power Gain and Efficiency at $f = 12.75$ GHz and

$V_{sig}(t) = 1.1 \sin \omega t - 0.191$ V. Large-Signal simulations of devices with w_T ranging from 2 μm to 5 μm and N_c from 2×10^{15} cm^{-3} to 1×10^{16} cm^{-3}, operating at 12.75 GHz and $V_{sig}(t) = 1.1 \sin \omega t - 0.191$ V were carried out and the results are summarized in Tables 5.8 and 5.9. It is observed that a maximum G_p of 18.61 dB at 29.9 percent efficiency is achieved by DEV:Si,n,B,6 x 10^{15},5 operating as a CATT amplifier as compared to a maximum G_p of 12.8 dB at 39-percent efficiency achieved by DEV:Si,n,B,2 x 10^{15},4 operating as a BJT amplifier. An additional 5.8-dB power gain at the expense of 10-percent efficiency reduction can be developed by employing a suitable CATT amplifier. If DEV:Si,n,B,6 x 10^{15},4 operating as a CATT amplifier is used, a 15.8-dB power gain at 38.5-percent efficiency can be achieved. Thus a well-designed CATT amplifier can achieve the same efficiency and a 3-dB additional power gain as compared to the maximum gain BJT amplifier at 12.75 GHz. The higher gain is mainly due to a multiplication factor of 1.72 and, to a lesser extent, a slightly larger allowed V_{RF}. If DEV:Si,n,B,6 x 10^{15},3 μm is operating as a CATT amplifier, a power gain of 12.3 dB can be achieved which is approximately the maximum power gain achievable by the BJT amplifier at 12.75 GHz. However, due to its shorter collector region, CATT amplifier DEV:Si,n,B,6 x 10^{15},3 has a higher efficiency than the maximum gain BJT amplifier.

It was noted previously that devices with $w_T \lesssim 2.5$ μm, when operating at optimum conditions and $f = 12.75$ GHz, are BJT amplifiers since their multiplication factors are less than 1.1. The BJT amplifiers

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with $w_T \lesssim 2.5$ μm have higher efficiencies but lower power gain than the CATT amplifiers.

5.4.2 Dynamic Range. The dynamic ranges of various CATT amplifiers and BJT amplifiers were investigated and the results are discussed in this section. The V_{bias} is kept constant at the optimum V_{bias} corresponding to $V_{sig}(t) = 1.1 \sin \omega t - 0.191$ V, although it was shown previously that the optimum V_{bias} varies slightly with the input signal level.

From Fig. 5.10 it is observed that G_p and η of both the CATT and BJT amplifiers are low at low input signal levels. This is due to low emitter injection efficiency at low input signal levels at an operating frequency of 12.75 GHz. At high input signal levels, G_p and η of both the CATT and BJT amplifiers deteriorate. In the case of CATT amplifiers, the deteriorations in G_p and η are due to space-charge-caused reductions in M_A and V_{RF} and space-charge-caused spreading in the induced current waveform. High injection level effects in the emitter-base region is another cause. In the case of BJT amplifiers, all the aforementioned are causes for reductions in G_p and η at higher input signal levels except the reduction in M_A. By definition, M_A is never greater than 1.1 for BJT amplifiers.

By comparing Figs. 5.10a and b, it is seen that DEV:Si,n,B,1 x 10^{16},4 has comparable G_p at low input signal levels, i.e., $P_{in} \lesssim 1$ x 10^{-3} W, as does DEV:Si,n,B,6 x 10^{15},4. Its G_p reduces faster with increasing P_{in} in the range 1 x 10^{-3} W $\lesssim P_{in} \lesssim 5$ x 10^{-3} W than that of DEV:Si,n,B,6 x 10^{15},4 due to the fact that M_A is a more important factor in determining its G_p and M_A is very sensitive to any space-charge-caused reduction in the electric field during emitter-base

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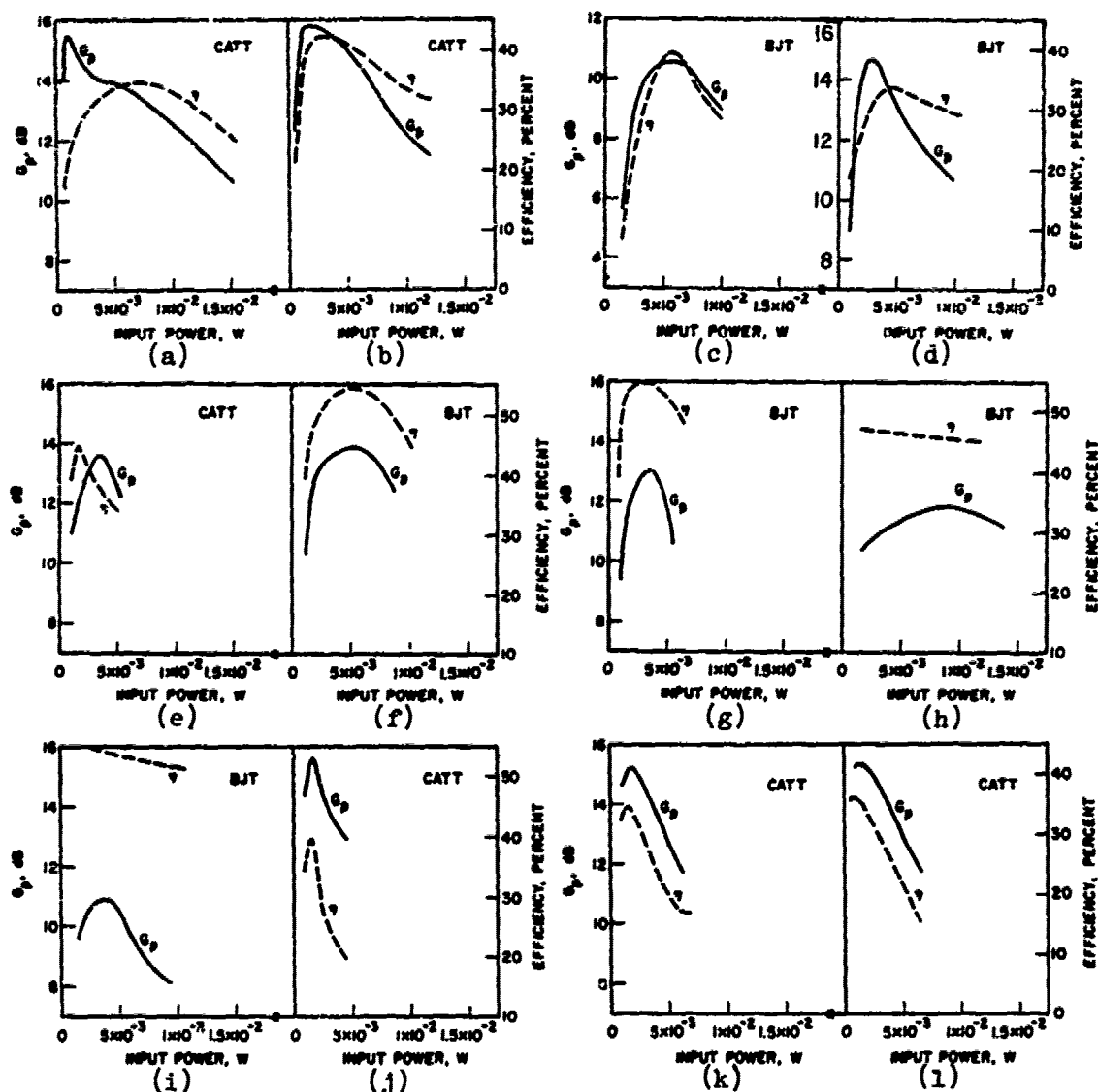
a. DEV:Si,n,B,1 x 10^{16},4; V$_{bias}$ = 51.5 V

b. DEV:Si,n,B,6 x 10^{15},4; V$_{bias}$ = 63.5 V

c. DEV:Si,n,B,6 x 10^{15},4; V$_{bias}$ = 35 V

d. DEV:Si,n,B,2 x 10^{15},4; V$_{bias}$ = 70 V

e. DEV:Si,n,B,6 x 10^{15},3; V$_{bias}$ = 56.5 V

f. DEV:Si,n,B,6 x 10^{15},3; V$_{bias}$ = 50 V

g. DEV:Si,n,B,2 x 10^{15},3; V$_{bias}$ = 45 V

h. DEV:Si,n,B,1 x 10^{16},2; V$_{bias}$ = 40 V

i. DEV:Si,n,B,2 x 10^{15},2; V$_{bias}$ = 33 V

j. DEV:Si,n,B,3 x 10^{16},0.6,2 x 10^{15},3.4; V$_{bias}$ = 65 V

k. DEV:Si,n,B,2.25x10^{16},0.8,2x10^{15},3.2; V$_{bias}$ = 65 V

l. DEV:Si,n,B,1.25x10^{16},1.2,2x10^{15},2.8; V$_{bias}$ = 65 V

FIG. 5.10   POWER GAIN AND EFFICIENCY VS. INPUT POWER

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charge injection. For $P_{in} > 5 \times 10^{-3}$ W, the rate of reduction in G_p is slower for DEV:Si,n,B,1 x 10^{16},4 because M_A is no longer as important in determining G_p and the space-charge effect in the low-field drift region of DEV:Si,n,B,1 x 10^{16},4 is not as severe as in DEV:Si,n,B,6 x 10^{15},4. This explains the even faster rate of reduction in G_p of DEV:Si,n,B,2 x 10^{15},4 as shown in Fig. 5.10d. Of the three devices with uniformly doped collectors, DEV:Si,n,B,6 x 10^{15},4 has the best G_p and η characteristics. All three devices with HI-LO collector structures, whose G_p and η characteristics are shown in Figs. 5.10j through l, are very inferior to DEV:Si,n,B,6 x 10^{15},4.

Devices whose G_p and η characteristics are shown in Figs. 5.10c, f and g through i are BJT amplifiers. It is observed that the amplifier dynamic range is severely reduced when N_c is too low (due to space-charge effects) and shorter devices with properly designed N_c have lower power gains but higher efficiencies and a wider dynamic range. The wide dynamic range associated with a short device, i.e., $w_T = 2$ μm, is due to the fact that $M_A \lesssim 1.1$ at optimum V_{bias} even at low input signal levels and therefore an almost constant M_A, independent of space charge, exists.

5.4.3 <u>Inherent</u> <u>Bandwidth</u>. Plots of G_p, η, V_{RF} and M_A vs. frequency for CATT and BJT amplifiers are shown in Figs. 5.11 through 5.13. The decrease in G_p for a short BJT amplifier, i.e., DEV:Si,n,B,6 x 10^{15},2, can be attributed to well-known causes such as the emitter-base RC frequency cutoff mechanism, base and collector time delay, and collector capacitor charging time. Since M_A is limited to 1.1 or less for the BJT, V_{RF} decreases slightly as frequency is increased. This is shown in Fig. 5.13. This decrease in V_{RF} also plays

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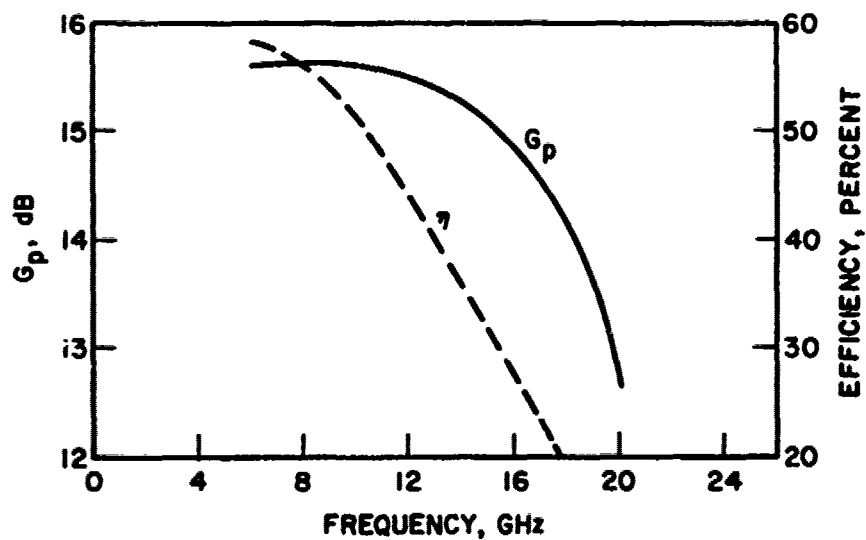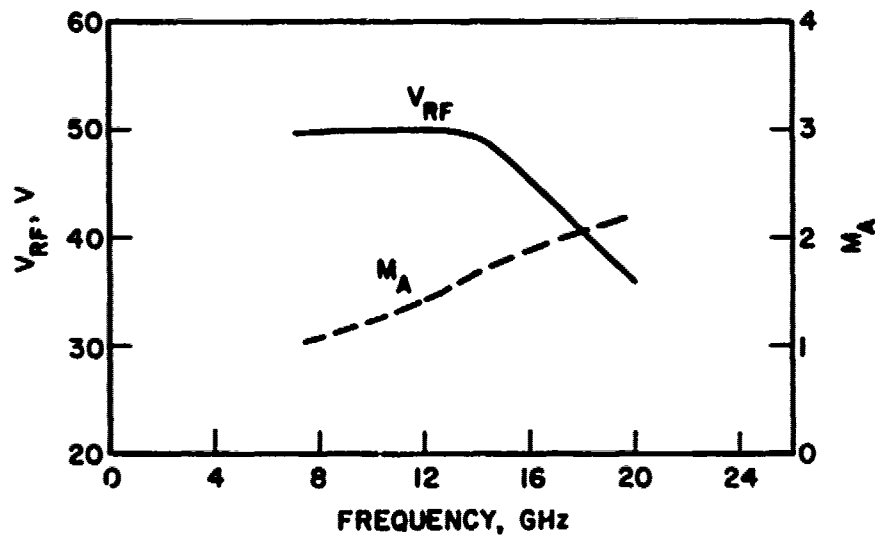
FIG. 5.11 CLASS C CATT AMPLIFIER PERFORMANCE VS. FREQUENCY

AT CONSTANT INPUT POWER LEVEL. (DEV:Si,n,B,6 x 10^{15},4

AND V_{bias} = 63.5 V)

FIG. 5.12 CLASS C BJT AMPLIFIER PERFORMANCE VS. FREQUENCY
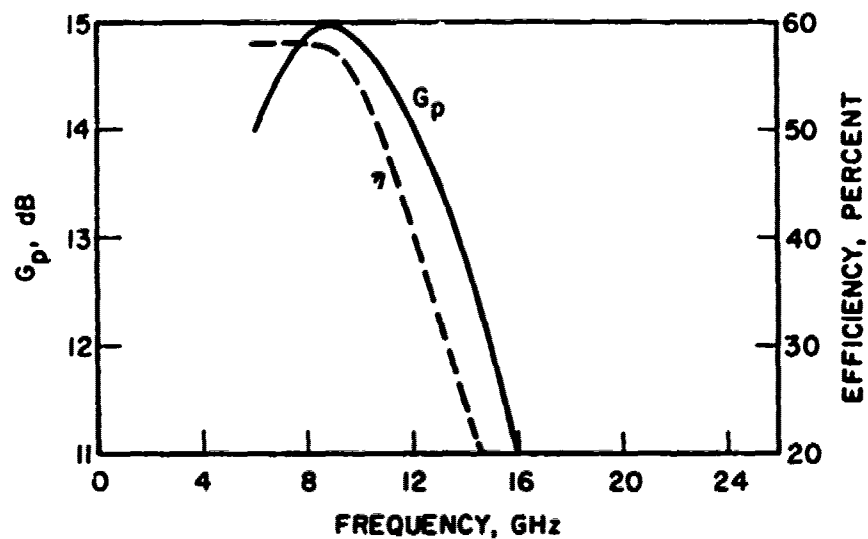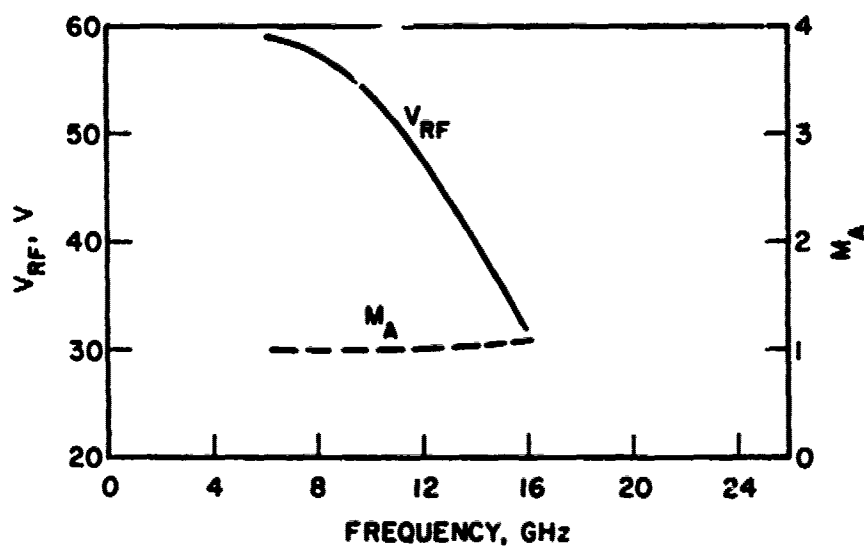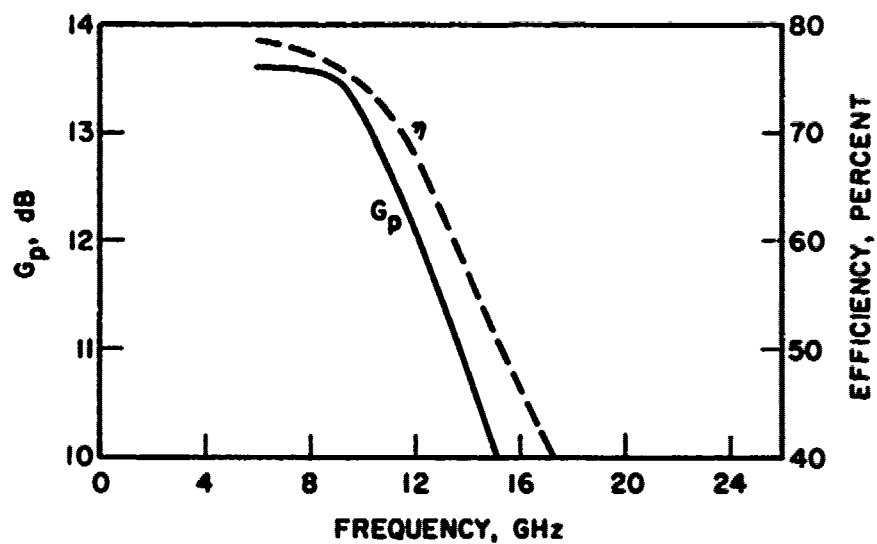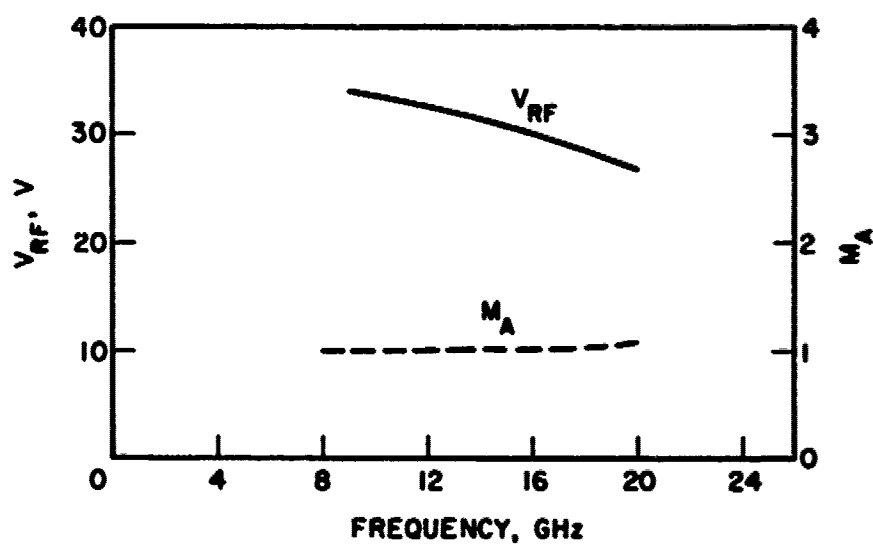AT CONSTANT INPUT POWER LEVEL. (DEV:Si,n,B,2 x 10^{15},4
AND V_{bias} = 70 V)

FIG. 5.13 CLASS C BJT AMPLIFIER PERFORMANCE VS. FREQUENCY

AT CONSTANT INPUT POWER LEVEL. (DEV:Si,n,B,6 x 10^{15},2

AND V_{bias} = 37.5 V)

a role in the decrease of G_p and η. For a longer BJT amplifier, i.e., DEV:Si,n,B,2 x 10^{15},4, the decrease in V_{RF} is more severe in order to keep $M_A \lesssim 1.1$. Thus, G_p and η decrease more rapidly with frequency as shown in Fig. 5.12. The inherent bandwidth of the 2-μm BJT is wider than the 4-μm BJT. For a CATT amplifier, M_A is allowed to take on any value as long as it is not too high and a stable operation cannot be achieved. The RF voltage amplitude V_{RF} of CATT device DEV:Si,n,B,6 x 10^{15},4 stays constant up to 14 GHz. For higher frequencies, V_{RF} decreases with increasing frequency in order to maintain stable operation. This decrease in V_{RF} results in decreases in G_p and η. As frequency increases, M_A also increases which helps to offset the decrease in G_p. This explains the slower rate of decrease in G_p as compared to that of η. The 4-μm CATT amplifier has a much wider inherent bandwidth than the 4-μm BJT amplifier.

5.5 Conclusions

Large-signal simulation results for both the Class C CATT and Class C BJT amplifier were presented in this chapter. The optimum dc bias condition, optimum load and their variations with frequency were investigated. The effects of device structural parameters were studied and optimum device structures for both the CATT and the BJT amplifier operating at 12.75 GHz were obtained. Several differences in the design of optimum CATT and BJT amplifiers were derived from the large-signal simulation results. Comparison between the CATT and the BJT amplifiers in terms of gain, efficiency, dynamic range and intrinsic bandwidth were also given.

CHAPTER VI.   SUMMARY, CONCLUSIONS, AND SUGGESTIONS
FOR FURTHER STUDY

6.1 Summary and Conclusions

The purpose of this study was to investigate the effects of avalanche multiplication and transit time in the collector region of a BJT. Analytical equations, circuit models, and computer simulations were used to determine dc, small-signal, and large-signal behavior of CATT amplifiers.

In Chapter II a dc computer program was developed which determines the dc avalanche multiplication factor vs. V_{bias} characteristics for any Si or GaAs collector structure. The results provide an estimation of device large-signal performance capability. The optimum collector parameters, i.e., w_{av}, N_{av}, N_c, obtained from the dc computer program correspond well to the results of large-signal simulation. Results also indicate that an n-type Si CATT amplifier is superior to p-type Si and n-type GaAs CATT amplifiers due to its favorable M_{A_o} vs. V_{bias} characteristics.

In Chapter III analytical models of dc and small-signal characteristics for CATT devices with Read-type collector structures were given which incorporated both the avalanche multiplication and the collector transit-time mechanisms. Contrary to previous findings, the small-signal characteristics of Class A CATT amplifiers indicated that a larger avalanche multiplication factor results in a smaller RF power gain and an increase in M_{A_o} does not necessarily imply a significant increase in f_{max}. Results were given and discussed. One conclusion was the inapplicability of CATT devices as Class A amplifiers.

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In Chapter IV a large-signal computer simulation was developed which incorporated several improvements over the large-signal simulation previously reported,[33] i.e., high injection level effects in the base region, Early effect, effect of high impurity level in the emitter, nonzero minority carrier concentration at the edge of the base-collector depletion region on the base side, minority carrier induced electric field in the base region, current conserving boundary condition for minority carriers in the collector region, and diffusion current in the collector depletion region.

In Chapter V large-signal results of Class C CATT amplifiers were given. Effects of base-collector dc bias, load, operating frequency and collector structures were examined and discussed. The simulation calculates output power, power gain, and efficiency of the amplifier. It also gives emitter-base current and voltage waveforms; avalanche multiplication factor; J_T and V_T waveforms; and spatial distributions of electrons, holes, and electric field in the collector depletion region at any time instant. Various Si n-type CATT and BJT Class C amplifiers operating at 12.75 GHz were compared in terms of output power, power gain, efficiency, and dynamic range. Optimum collector impurity doping level and optimum width of the collector region of both the CATT and BJT amplifiers were determined and discussed. Carrier multiplication and long collector transit time do increase power gain, but at the expense of lower efficiency and smaller dynamic range. Avalanche multiplication does help to increase the device inherent bandwidth.

6.2 Suggestions for Further Study

In the course of this study several additional topics which need further exploration were found. They are as follows:

1. A cost-tolerable, two-dimensional, large-signal computer simulation program to account for the nonuniform injection of carriers at the emitter-base junction and the nonuniform injection of carriers into the collector region due to nonuniform emitter-base junction potential across the emitter finger laterally caused by the flow of conventional base current and feedback hole current in a resistive base region.

2. Fabrication of X-band CATT devices and experimental studies of Class C CATT amplifiers.

3. Construction of new models for use at higher frequencies.

4. Small-signal and large-signal noise theories for CATT devices.

5. Thermal limitation studies.

6. Application of CATT devices as high-voltage, high-current drivers.

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